乐升半导体
LEVETOP

# LT7589

*High Performance Uart TFT Display Controller*

# Brief Specification

**V1.3**

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Levetop Semiconductor Co., Ltd.

# Version History

| Version | Release Date | Description |
|---|---|---|
| V1.0 | 2024/10/29 | ● LT7589 Preliminary Release |
| V1.0A | 2024/12/30 | ● Update Application Circuit |
| V1.1 | 2025/03/20 | ● Update Pin - VDD33_IO Description<br>● Update Application Circuit |
| V1.2 | 2025/04/21 | ● Modify the pin signal description of “LCD_XI”<br>● Update Table 6-4 External Flash Signal Description<br>● Update Application Circuit |
| V1.3 | 2025/11/28 | ● Table 8-1: QFN-96Pin Dimensions<br>● Figure9-2: LT7589B Application Circuit |

# Copyright

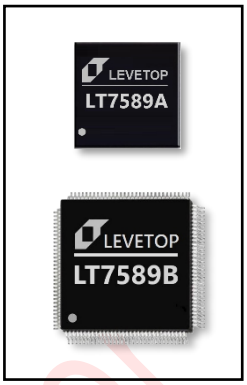
# Content

# Figure List



# Table List

# 1. Chip Introduction




LT7589 is a high-performance Serial Uart TFT Panel Controller. Internally integrated with a 32-bit RISC MCU and a GUI (Graphic User Interface) with TFT LCD graphics display controller, the main function is to provide Uart serial communication, allowing the main control MCU to easily present the information to be displayed on the TFT panel through simple serial commands. The internal hardware of LT7589 also provides JPG image decoding PIP (Picture-in-Picture), Geometric drawing and other functions can improve the display efficiency of TFT panel and reduce the time required for MCU to process graphic displays. The LT7589 supports display resolutions ranging from 480 * 480 (QVGA) to 1280 * 800, suitable for 16/24bit RGB interface TFT displays.

The internal MCU of LT7589 has a maximum clock frequency of 200MHz, contains 2MB Flash, 768KB SRAM, 16MB display memory, and is combined with JPG decoder, 2D graphics acceleration display, DMA data reading, and high-speed QSPI Flash interface to quickly read images, animations, word libraries, and other information stored in external QSPI Flash, with good display performance. LT7589 can be used in conjunction with UI editing software (UI-Editor) and simulation software (UI-Emulator) developed by Levetop Semiconductor to directly import and develop display interfaces for designed UI materials and display interaction logic on a computer. Its supported display functions include image display, animation display, sliding menu display, progress bar display, string display, Chinese English keyboard, numeric keyboard, analog clock, digital clock, pointer display, QR code generation, multi language, audio playback, variable control, and control effects combined with touch screen or encoder functions. In addition to the serial port screen Uart communication interface, LT7589 also provides multiple sets of SCI (Uart) interfaces to connect components such as Bluetooth modules, WiFi modules, etc. It also offers CanBus, SD card (SPI mode), analog input AIN, PWM, and INT interrupt interfaces, and comes with an RTC clock. It can also be used for GUI graphic development in Little VGL, with good fluency and high cost-effectiveness.

Due to its high capacity of Flash and SRAM, the LT7589 can also be used as a main control MCU with a TFT controller, completing the main control and TFT display functions with one LT7589. Its display function is very suitable for electronic products with TFT-LCD panels below 1280x800 resolution, or to replace the original monochrome panel products, enhancing the product's intelligent display of information, increasing product quality and grade. The powerful display function of LT7589 is very suitable for use in electronic products with TFT-LCD panels, such as various smart home appliances, car dashboards, motorcycle panels, multifunctional transaction machines, industrial controls, electronic instruments, medical beauty equipment, testing equipment, charging equipment, inverters, UPS and other power equipment, audio equipment, as well as smart speakers with TFT panel, robots and other products.

# 2. Application Block Diagram

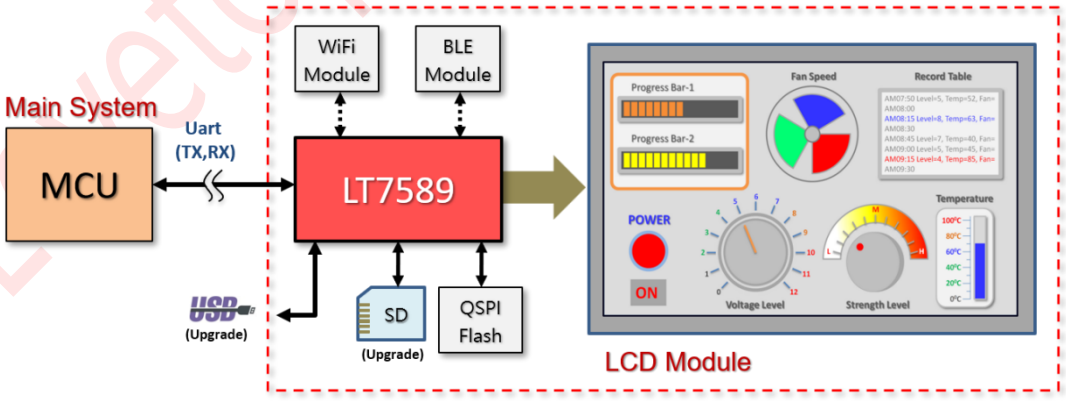



**Figure 2-1: LT7589 Designed on TFT Module**

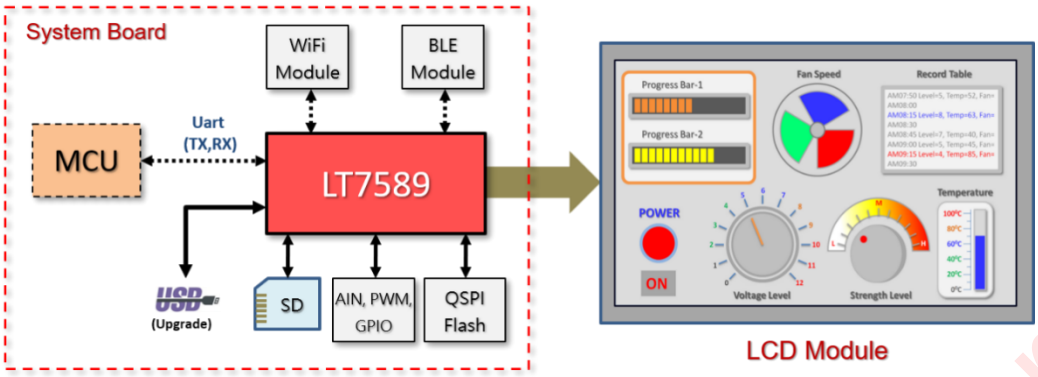



Figure 2-2: LT7589 Designed on System Board

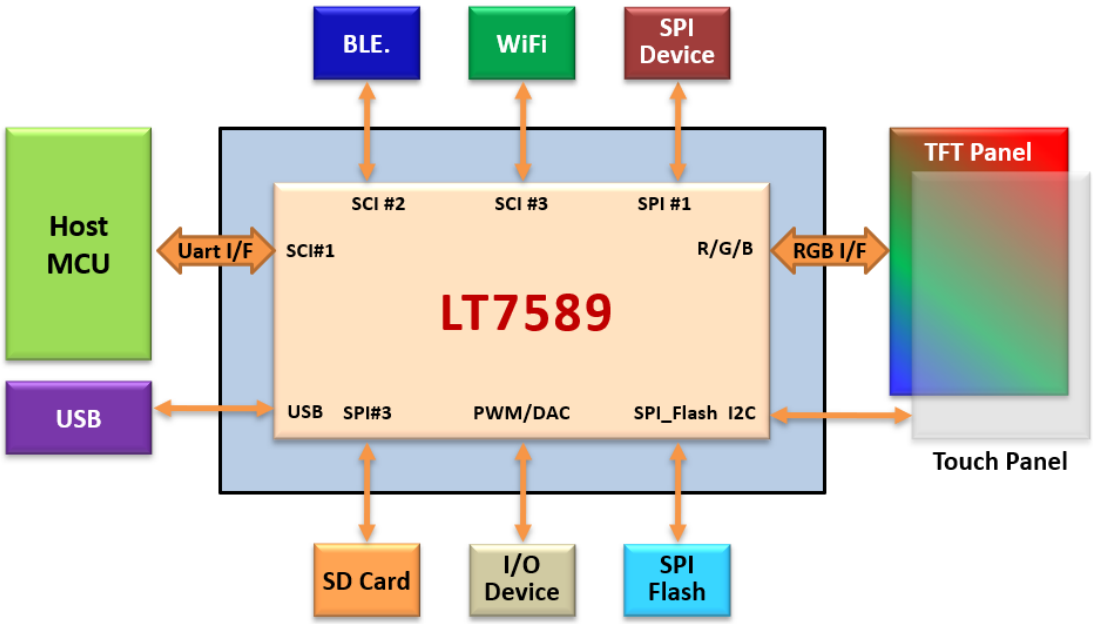



Figure 2-3: LT7589 Application Architecture

## 3. Internal Block Diagram

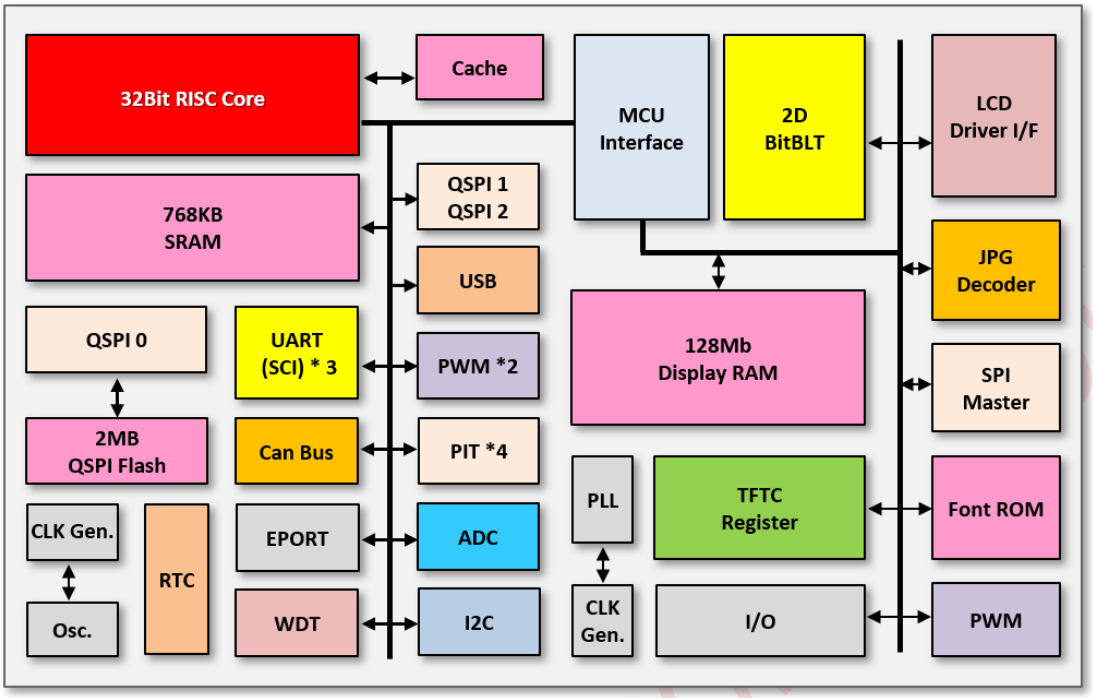



**Figure 3-1: LT7589 Internal Block Diagram**

**Table 3-1: Part Number**

| Model | Package | Display RAM | Resolution | Colors |
|---|---|---|---|---|
| LT7589A | QFN-96 | 128Mb | 1280*800 | 16.7M Color αRGB 8:8:8:8 |
| LT7589B | LQFP-128 | 128Mb | 1280*800 | 16.7M Color αRGB 8:8:8:8 |

# 4. Features

## Host MCU Interface

- Support Uart, USB Interface
- Embedded 32Bit MCU, main clock is 180MHz, and 200MHz for max.

## USB Interface

- Support USB2.0 Full Speed。

## SCI (Uart) Interface

- Supports Three SCI (Serial Communications Interface)
- Components or modules that can be connected to external SCI interfaces

## Memory

- MCU Embedded 2M bytes Flash
- MCU Embedded 512K+256K bytes SRAM
- TFT Controller Embedded 128Mbit Display RAM

## Display Data Format

- 16bpp: Color RGB 5:6:5 (2bytes/pixel)
- 24bpp: Color RGB 8:8:8 (3bytes/pixel)
  - αRGB 4:4:4:4 ( 4,096 Index color/pixel, including transparency attribute)
- 32bpp : Color αRGB 8:8:8:8 (4bytes/pixel)

## Panel Interface and Resolution

- Supports 16 or 24bits RGB Interface Panel
- Supported resolutions for bare metal development:
  - VGA : 640*480 TFT Panel
  - WVGA : 800*480 TFT Panel
  - SVGA : 800*600 TFT Panel
  - XGA : 1024*768 TFT Panel
  - SXGA : 1280*1024 TFT Panel
- Maximum resolution supported during serial TFT panel development: 1280*800

## Geometry Display accelerator

- Provide drawing functions such as drawing points, lines, curves, ellipses, triangles, rectangles, rounded rectangles, etc

## Display Functions

- Built in JPG hardware decoder
- Support users to define four 32*32 graphic cursor options.
- Provide virtual display function: Virtual display can display images larger than the size of the LCD panel, so that the images can easily scroll in any direction.
- Provide Picture in Picture (PIP) display: Supports two PIP window regions: the enabled PIP window is displayed above the main window, while the PIP1 window is displayed above the PIP2 window.
- Support multiple display functions: You can switch the main display window between display buffers to achieve simple animation display effects.
- Support the function of quickly displaying images when awakened.
- Supports mirroring and vertical flipping display functions.
- Color Bar Display: It can still be displayed in ribbon format without writing data to the internal display memory, with a default resolution of 640 * 480 pixels.

## BitBLT Engine

- Built in 2D BitBLT engine.
- Provide the function of copying images with raster operation.
- Provide color depth conversion.
- Solid filling and pattern filling functions:
  - Provide user-defined 8*8 images or 16*16 images.
- Provide the function of combining two images into one image:
  - Chroma Keying function: Mix the image with specified RGB colors based on transparency
  - Window Alpha blending mode: Mix two images based on the transparency within the specified area.
  - Pixel blending transparency mode (Dot Alpha blending): Mix two images based on RGB format and transparency.

## Display Text Mode

- Built in ISO/IEC 8859-1/2/4/5 font sizes of 8*16, 12*24, and 16*32
- Support users to customize half shaped character angles and full shaped characters (8*16, 12*24, 16*32, 16*16, 32*32).
- Supports full font sizes of 48*48 and 72*72
- Provide programmable text cursor.
- Supports vertical and horizontal font enlargement (*1, *2, *3, *4x).
- Supports 90 degree rotation of text

## SPI Master Interface

- The TFT graphics accelerator provides external serial flash data copying to the frame buffer.
- Compatible with standard QSPI specifications NOR/NAND Flash.
- Support bad block handling in Nand Flash.
- Support MCU to use Pass Mode for SPI Flash.
- Provide 16 bytes read FIFO and 16 bytes write FIFO.
- When the Tx FIFO is completely cleared and the SPI Tx/Rx engine is idle, an interrupt will be issued.
- Provide 2 additional sets of compatible standard SPI interfaces.

## I2C Interface

- MCU provides I2C interface to connect with external I2C devices
- Provide standard transmission mode (100kbps) and fast transmission mode (400kbps)

## PWM Interface

- MCU provides 8 PWM interfaces
- The TFT controller has two built-in 16bit counters and provides two PWM output interfaces
- Programmable operation cycle

## Interrupt Signals

- MCU can provide up to 19 interrupt input
- The TFT controller provides an interrupt output interface.

## GPIO

- MCU can provide up to 24 GPIO Port
- The TFT controller can provide up to 17 GPIO Port

## Analog Input

- MCU Supports eight ADC Analog Input

## Reset

- MCU provides power on reset, external reset input, software reset, watchdog reset, and voltage detection reset
- The TFT controller provides power on reset, external hardware reset, and software command reset

## Power Saving Mode

- Support Standby mode, Suspend mode and Sleep Mode
- Support MCU wake up

## Clock

- MCU and TFT controller have independent clocks.
- MCU built-in precise high-frequency clock
- Built in RTC and external 32KHz crystal oscillator circuit.
- TFT controller with built-in programmable PLL, providing internal clock, external LCD clock, and internal display memory clock

## Power Supply

- VDD Power: 3.3V +/- 0.3V
- Embedded 1.2V LDO

## Package Type

- QFN-96Pin (10*10mm$^2$)
- LQFP-128Pin (14*14mm$^2$)

## Operation Temp.

- -40℃~85℃。(@180MHz)

# 5. Pin Assignment

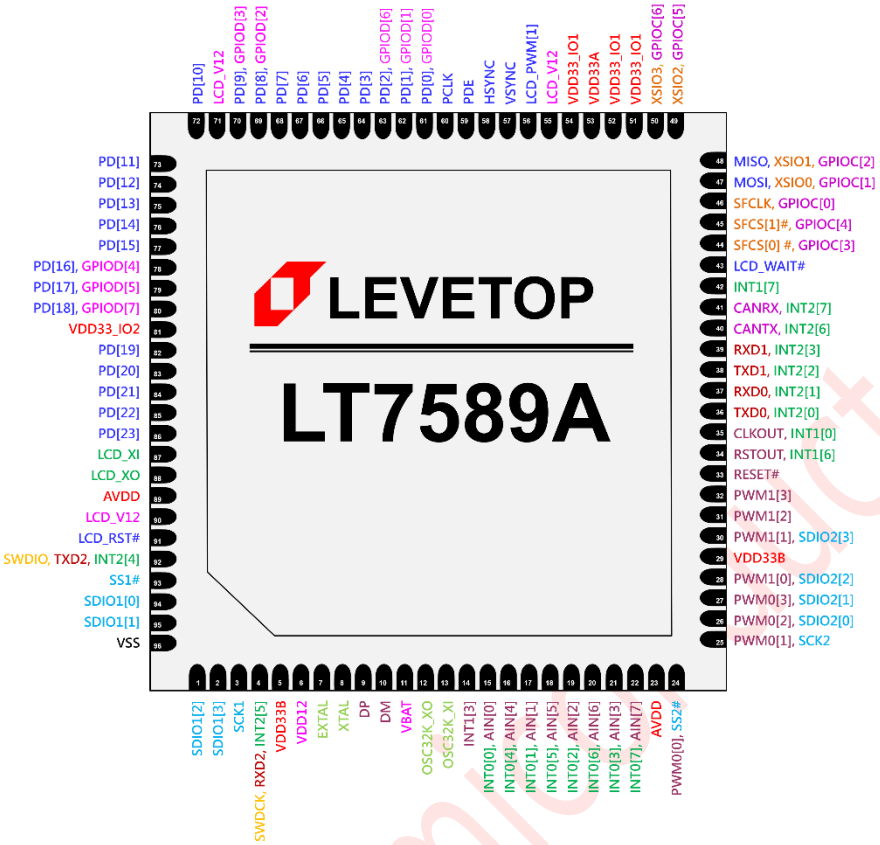



**Figure 5-1: LT7589A Pin Assignment (QFN-96Pin)**

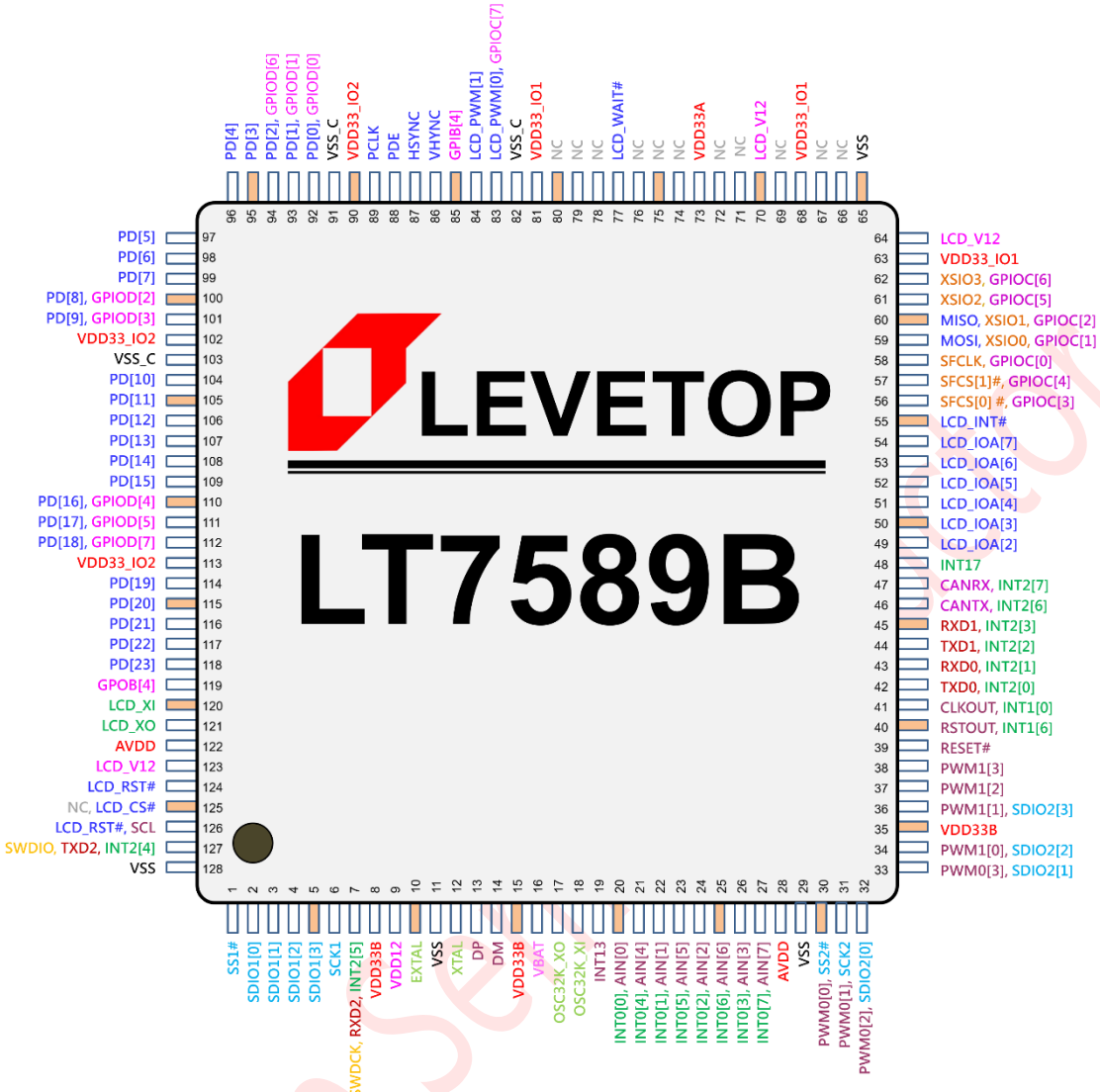



**Figure 5-2: LT7589B Pin Assignment (LQFP-128Pin)**

# 6. Pin Description

## 6.1 SCI (Uart) Signals

**Table 6-1: SCI (Uart) Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 37 | 43 | RXD0 | I | **Serial Communication (Uart) #0 Receives Data Input**<br>This signal is used for SCI #0 receiver data input and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[1]. |
| 36 | 42 | TXD0 | O | **Serial communication (Uart) #0 Transmission Data Output**<br>This signal is used for SCI #0 transmitter data output and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[0]. |
| 39 | 45 | RXD1 | I | **Serial Communication (Uart) #1 Receives Data Input**<br>This signal is used for SCI #1 receiver data input and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[3]. |
| 38 | 44 | TXD1 | O | **Serial communication (Uart) #1 Transmission Data Output**<br>This signal is used for SCI #1 transmitter data output and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[2]. |
| 4 | 7 | RXD2 | I | **Serial Communication (Uart) #2 Receives Data Input**<br>This signal is used for SCI #2 receiver data input and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[5]. |
| 92 | 127 | TXD2 | O | **Serial communication (Uart) #2 Transmission Data Output**<br>This signal is used for SCI #2 transmitter data output and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[4]. |

## 6.2 LCD Panel Signals

**Table 6-2: LCD Panel Signals**

<table>
<tr><th>Pin # LT7589A</th><th>Pin # LT7589B</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>86~82,<br>80~72,<br>70~61</td><td>118~114,<br>112~104,<br>101~92</td><td>PD[23:19],<br>PD[18:10],<br>PD[9:0]</td><td>O</td><td>LCD Panel Data Bus<br>TFT LCD data bus output for source driver. User can connect to corresponding RGB bus for different settings.
<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">TFT-LCD Interface</th></tr>
<tr><th>16bits</th><th>24bits</th></tr>
<tr><td>PD[0]</td><td>GPIOD[0]</td><td>B0</td></tr>
<tr><td>PD[1]</td><td>GPIOD[1]</td><td>B1</td></tr>
<tr><td>PD[2]</td><td>GPIOD[6]</td><td>B2</td></tr>
<tr><td>PD[3]</td><td>B0</td><td>B3</td></tr>
<tr><td>PD[4]</td><td>B1</td><td>B4</td></tr>
<tr><td>PD[5]</td><td>B2</td><td>B5</td></tr>
<tr><td>PD[6]</td><td>B3</td><td>B6</td></tr>
<tr><td>PD[7]</td><td>B4</td><td>B7</td></tr>
<tr><td>PD[8]</td><td>GPIOD[2]</td><td>G0</td></tr>
<tr><td>PD[9]</td><td>GPIOD[3]</td><td>G1</td></tr>
<tr><td>PD[10]</td><td>G0</td><td>G2</td></tr>
<tr><td>PD[11]</td><td>G1</td><td>G3</td></tr>
<tr><td>PD[12]</td><td>G2</td><td>G4</td></tr>
<tr><td>PD[13]</td><td>G3</td><td>G5</td></tr>
<tr><td>PD[14]</td><td>G4</td><td>G6</td></tr>
<tr><td>PD[15]</td><td>G5</td><td>G7</td></tr>
<tr><td>PD[16]</td><td>GPIOD[4]</td><td>R0</td></tr>
<tr><td>PD[17]</td><td>GPIOD[5]</td><td>R1</td></tr>
<tr><td>PD[18]</td><td>GPIOD[7]</td><td>R2</td></tr>
<tr><td>PD[19]</td><td>R0</td><td>R3</td></tr>
<tr><td>PD[20]</td><td>R1</td><td>R4</td></tr>
<tr><td>PD[21]</td><td>R2</td><td>R5</td></tr>
<tr><td>PD[22]</td><td>R3</td><td>R6</td></tr>
<tr><td>PD[23]</td><td>R4</td><td>R7</td></tr>
</table>
When the LCD is set to 16/18bpp function mode, some PDs can be defined as GPIO pins.</td></tr>
<tr><td>60</td><td>89</td><td>PCLK</td><td>O</td><td>Pixel Clock<br>Generic TFT interface signal for panel scan clock. It derives from internal PLL.</td></tr>
</table>

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 57 | 86 | VSYNC | O | **VSYNC Pulse Signal**<br>Generic TFT interface signal for vertical synchronous pulse. |
| 58 | 87 | HSYNC | O | **HSYNC Pulse Signal**<br>Generic TFT interface signal for horizontal synchronous pulse. |
| 59 | 88 | PDE | O | **Data Enable Signal**<br>Generic TFT interface signal for data valid or data enable. |

## 6.3 QSPI Signals

**Table 6-3: QSPI Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 3 | 6 | SCK1 | O | **QSPI #1 Serial Clock Signal**<br>This signal is the clock signal output of the first group SPI and can be used to connect components or modules of external SPI interfaces. |
| 93 | 1 | SS1# | O | **QSPI #1 Chip Selection Signal**<br>This signal is the chip selection output of the first group SPI. |
| 94 | 2 | SDIO1[0] | IO | **Data Output/Input Signal of QSPI #1**<br>This signal is the output/input signal of the first group QSPI data 0. |
| 95 | 3 | SDIO1[1] | IO | **Data Output/Input Signal of QSPI #1**<br>This signal is the output/input signal of the first group QSPI data 1. |
| 1 | 4 | SDIO1[2] | IO | **Data Output/Input Signal of QSPI #1**<br>This signal is the output/input signal of the first group QSPI data 2. |
| 2 | 5 | SDIO1[3] | IO | **Data Output/Input Signal of QSPI #1**<br>This signal is the output/input signal of the first group QSPI data 3. |
| 25 | 31 | SCK2<br>PWM0[1] | O | **QSPI #2 Serial Clock Signal**<br>This signal is the clock signal output of the second group SPI and can be used to connect components or modules of external SPI interfaces.<br>This pin shares with pin PWM0[1]. |
| 24 | 30 | SS2#<br>PWM0[0] | O | **QSPI #2 Chip Selection Signal**<br>This signal is the chip selection output of the second group SPI.<br>This pin shares with pin PWM0[0]. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 26 | 32 | SDIO2[0]<br>PWM0[2] | IO | **Data Output/Input Signal of QSPI #2**<br>This signal is the output/input signal of the second group QSPI data 0.<br>This pin shares with pin PWM0[2]. |
| 27 | 33 | SDIO2[1]<br>PWM0[3] | IO | **Data Output/Input Signal of QSPI #2**<br>This signal is the output/input signal of the second group QSPI data 1.<br>This pin shares with pin PWM0[3]. |
| 28 | 34 | SDIO2[2]<br>PWM1[0] | IO | **Data Output/Input Signal of QSPI #2**<br>This signal is the output/input signal of the second group QSPI data 2.<br>This pin shares with pin PWM1[0]. |
| 30 | 36 | SDIO2[3]<br>PWM1[1] | IO | **Data Output/Input Signal of QSPI #2**<br>This signal is the output/input signal of the second group QSPI data 3.<br>This pin shares with pin PWM1[1]. |

## 6.4 External Flash Signals

**Table 6-4: External Flash Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 45 | 57 | SFCS[1]#<br>GPIOC[4] | IO | **External Serial Flash #1 Chip Selection Signal**<br>This signal is controlled by the LCD controller inside LT7589. If the serial QSPI function is disabled, this pin can be set to GPOC[4], which defaults to input function.<br>**Note:**<br>Under the serial panel function framework of Levetop Semiconductor, only SFCS[1]# is allowed to be used as the chip selection signal for external QSPI Flash, and SFCS[0]# cannot be used. |
| 44 | 56 | SFCS[0]#<br>GPIOC[3] | IO | **External Serial Flash #0 Chip Selection Signal**<br>This signal is controlled by the LCD controller inside LT7589. If the serial QSPI function is disabled, this pin can be set to GPOC[3], which defaults to input function.<br>**Note:**<br>Under the serial panel function framework of Levetop Semiconductor, this signal cannot be used as the chip selection signal for external QSPI Flash, and SFCS[1]# must be used. SFCS[0]# can only be used when the customer develops it with own code. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 46 | 58 | SFCLK<br>GPIOC[0] | IO | **External Serial Flash Clock Signal**<br>This pin is a serial clock signal output, controlled by the LCD controller inside LT7589, and connected to external Serial Flash or QSPI components.<br>If the serial QSPI function is disabled, this pin can be set to GPOC[0] and default to input function. |
| 47 | 59 | XSIO0<br>GPIOC[1] | IO | **QSPI Data Input/Output Signal 0**<br>This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component.<br>If the serial SPI function is disabled, this pin can be set to GPOC[1] and default to input function. |
| 48 | 60 | XSIO1<br>GPIOC[2] | IO | **QSPI Data Input/Output Signal 1**<br>This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component.<br>If the serial SPI function is disabled, this pin can be set to GPOC[2] and default to input function. |
| 49 | 61 | XSIO2<br>GPIOC[5] | IO | **QSPI Data Input/Output Signal 2**<br>This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component.<br>If the serial SPI function is disabled, this pin can be set to GPOC[5] and default to input function. |
| 50 | 62 | XSIO3<br>GPIOC[6] | IO | **QSPI Data Input/Output Signal 3**<br>This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component.<br>If the serial SPI function is disabled, this pin can be set to GPOC[6] and default to input function. |

## 6.5 PWM Signals

**Table 6-5: PWM Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| -- | 83 | LCD_PWM[0]<br>GPIOC[7] | IO | **LCD PWM#0 Output Signal**<br>This signal is controlled by the register of the LCD controller inside LT7589, and is a programmable PWM output signal that can be used to control the backlight or other components of the TFT LCD screen. The output mode of LCD_PWM can be set through the registers of the LCD controller.<br>This pin shares with pin GPOC[7]. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 56 | 84 | LCD_PWM[1] | IO | **LCD PWM#1 Output Signal**<br>This signal is controlled by the register of the LCD controller inside LT7589, and is a programmable PWM output signal that can be used to control the backlight or other components of the TFT LCD screen. The output mode of LCD_PWM [1] can be set through the registers of the LCD controller. |
| 24 | 30 | PWM0[0]<br>SS2# | IO | **The PWM0[0] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers.<br>This pin shares with pin SS2#. |
| 25 | 31 | PWM0[1]<br>SCK2 | IO | **The PWM0[1] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers.<br>This pin shares with pin SCK2. |
| 26 | 32 | PWM0[2]<br>SDIO2[0] | IO | **The PWM0[2] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers.<br>This pin shares with pin SDIO2[0]. |
| 27 | 33 | PWM0[3]<br>SDIO2[1] | IO | **The PWM0[3] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers.<br>This pin shares with pin SDIO2[1]. |
| 28 | 34 | PWM1[0]<br>SDIO2[2] | IO | **The PWM1[0] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers.<br>This pin shares with pin SDIO2[2]. |
| 30 | 36 | PWM1[1]<br>SDIO2[3] | IO | **The PWM1[1] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers.<br>This pin shares with pin SDIO2[3]. |
| 31 | 37 | PWM1[2] | IO | **The PWM1[2] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers. |
| 32 | 38 | PWM1[3] | IO | **The PWM1[3] Output Signal Controlled by MCU**<br>Can be used as PWM output or GPIO, set by internal MCU registers. |

## 6.6 USB Signals

**Table 6-6: USB Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 9 | 13 | DP | IO | **USB Data Port (Positive)**<br>This is the signal of USB data terminal DP. |
| 10 | 14 | DM | IO | **USB Data Port (Negative)**<br>This is the signal of USB data terminal DM. |

## 6.7 GPIO and Interrupt Signals

**Table 6-7: GPIO and Interrupt Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 15 | 20 | INT0[0]<br>AIN[0] | I | **Interrupt INT0[0] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 17 | 22 | INT0[1]<br>AIN[1] | I | **Interrupt INT0[1] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 19 | 24 | INT0[2]<br>AIN[2] | I | **Interrupt INT0[2] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 21 | 26 | INT0[3]<br>AIN[3] | I | **Interrupt INT0[3] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 16 | 21 | INT0[4]<br>AIN[4] | I | **Interrupt INT0[4] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 18 | 23 | INT0[5]<br>AIN[5] | I | **Interrupt INT0[5] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 20 | 25 | INT0[6]<br>AIN[6] | I | **Interrupt INT0[6] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 22 | 27 | INT0[7]<br>AIN[7] | I | **Interrupt INT0[7] Signal**<br>Can be used as an interrupt input or as an analog signal input. |
| 36 | 42 | INT2[0]<br>TXD0 | I | **Interrupt INT2[0] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin TXD0. |
| 37 | 43 | INT2[1]<br>RXD0 | IO | **Interrupt INT2[1] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin RXD0. |
| 38 | 44 | INT2[2]<br>TXD1 | I | **Interrupt INT2[2] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin TXD1. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 39 | 45 | INT2[3]<br>RXD1 | IO | **Interrupt INT2[3] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin RXD1. |
| 92 | 127 | INT2[4]<br>TXD2 | I | **Interrupt INT2[4] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin TXD2. |
| 4 | 7 | INT2[5]<br>RXD2 | IO | **Interrupt INT2[5] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin RXD2. |
| 40 | 46 | INT2[6]<br>CANTX | I | **Interrupt INT2[6] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin CANTX. |
| 41 | 47 | INT2[7]<br>CANRX | IO | **Interrupt INT2[7] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin CANRX. |
| 35 | 41 | INT1[0]<br>CLKOUT | IO | **Interrupt INT1[0] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin CLKOUT. |
| 14 | 19 | INT1[3] | IO | **Interrupt INT1[3] Signal**<br>Can be used as an interrupt input. |
| 34 | 40 | INT1[6]<br>RSTOUT | IO | **Interrupt INT1[6] Signal**<br>Can be used as an interrupt input.<br>This pin shares with pin RSTOUT. |
| 42 | 48 | INT1[7] | IO | **Interrupt INT1[7] Signal**<br>Can be used as an interrupt input. |
| -- | 55 | LCD_INT# | O | **LCD Interrupt Output Signal**<br>When the interrupt condition set by the LCD controller occurs, this pin becomes low and is used to generate an interrupt output to inform the MCU. |
| --, 50, 49, 45, 44, 48, 47, 46 | 83, 62, 61, 57, 56, 60, 59, 58 | GPIOC[7]<br>GPIOC[6:0] | IO | **GPIO Output/Input Signals of LCD Controller**<br>These signals are controlled by the register of the LCD controller inside LT7589, and the output data of GPOC[7] shares pins with LCD_PWM[0].<br>GPOC [6:0] shares pins with {XSIO3, XSIO2, SFC[1] #, SFC[0] #, XSIO1, XSIO0, SFCLK} and can only be used when the functions of LCD_PWM and SPI Master are disabled. The output mode of these pins can be set through the registers of the TFT LCD controller. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 80, 63, 79, 78, 70, 69, 62, 61 | 112, 94, 111, 110, 101, 100, 93, 92 | GPIOD[7:0] | IO | **GPIO Output/Input Signals of LCD Controller**<br>These signals are controlled by the register of the LCD controller inside LT7589, and the output data of GPOD [7:0] shares pins with {PD[18], PD[2], PD[17], PD[16], PD[9], PD[8], PD[1], PD[0]}.<br>GPOD[7:0] can only be used when the LCD panel data bus is set to 16 bits. The output mode of these pins can be set through the registers of the TFT LCD controller. |
| -- | 54~49 | LCD_IOA[7:2] | IO | **GPIO Output/Input Signals of LCD Controller**<br>The output/input modes of these pins can be set through the registers of the TFT LCD controller. |

## 6.8 ADC Input Signals

**Table 6-8: ADC Input Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 22, 20, 18, 16, 21, 19, 17, 15 | 27, 25, 23, 21, 26, 24, 22, 20 | AIN[7:0]<br>INT0[7:0] | IO | **Analog Input Signals**<br>These analog signals are used as ADC analog input channels. When not configured as analog inputs, these signals can also be used for INT0[7:0]. |

## 6.9 Miscellaneous Signals

**Table 6-9: Miscellaneous Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 43 | 77 | LCD_WAIT# | O | **Waiting for Output Signal**<br>When the internal MCU performs read and write control on the LCD control circuit, if it is in a busy state, WAIT # will be set to a low potential to inform the MCU to enter the waiting cycle. |
| -- | 125 | LCD_CS#<br>NC | I | **LCD Control Circuit Chip Selection Signal**<br>LCD_CS# = 0, Represents the command or data read/write cycle of the internal MCU to the LCD control circuit.<br>Note: This pin has already been internally connected to the EBI-CS # of the MCU and must be kept in NC. |
| 91 | 124 | LCD_RST# | I | **Reset Input Signal for LCD Control Circuit**<br>When RST #=0 and maintains a length greater than 32 clock cycles, LT7586 will generate a reset action. |
| -- | 126 | SCL<br>LCD_RST# | IO | **I2C Clock Signal**<br>This signal is used as the clock signal for I2C of MCU or GPIO.<br>Note: This pin should be connected to the LCD_RST# of Pin-124 to control whether the LCD circuit performs a reset action. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 4 | 7 | SWDCK<br>RXD2, INT2[5] | I | **Flash Programming Clock Signal**<br>This input signal is the clock signal used for programming internal flash memory.<br>This pin is also connected to RXD2 and INT2[5], it's a shared pin. |
| 92 | 127 | SWDIO<br>TXD2, INT2[4] | I | **Flash Programming Data Signal**<br>This input signal is used as a data signal for programming internal flash memory.<br>This pin is also connected to TXD2 and INT2[4], it's a shared pin. |
| 35 | 41 | CLKOUT<br>INT1[0] | O | **System Clock Signal Output**<br>This output signal reflects the internal system clock.<br>When not configured as a clock output, this signal can also be used for INT1[0]. |
| 34 | 40 | RSTOUT<br>INT1[6] | O | **MCU Reset Output Signal**<br>This output signal indicates that the internal reset controller is resetting the chip.<br>0 = The chip is in a reset state<br>1 = chip not reset state<br>When not configured as a reset output, this signal can also be used for INT1[6]. |
| 33 | 39 | RESET# | I | **MCU Reset Input Signal**<br>When RESET#=0, a reset action will be performed on the internal MCU. |

## 6.10 Power and Clock Signals

**Table 6-10: Power and Clock Signals**

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 87 | 120 | LCD_XI | I | **LCD Crystal/Clock Signal Input**<br>This pin is connected to an external crystal oscillator and serves as the input signal for the crystal oscillator circuit of the internal TFT LCD controller. When using an active crystal oscillator or an external clock signal, it can be input through this pin. Typically, this clock signal is connected to pin " XTAL", and the recommended crystal oscillator frequency (OSC) is 12MHz. |
| 88 | 121 | LCD_XO | O | **LCD Crystal Output**<br>This pin is connected to an external crystal oscillator and outputs a signal to the crystal oscillator circuit of the internal TFT controller. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 13 | 18 | OSC32K_XI | I | **32.768Khz Crystal Oscillator Input**<br>RTC clock signal, this pin is connected to an external 32.768Khz crystal oscillator. |
| 12 | 17 | OSC32K_XO | O | **32.768Khz Crystal Oscillator Output**<br>RTC clock signal, this pin is connected to an external 32.768Khz crystal oscillator. |
| 8 | 12 | XTAL | I | **USB Clock Signal**<br>This pin is connected to an external 12MHz crystal oscillator. |
| 7 | 10 | EXTAL | O | **USB Clock Signal**<br>This pin is connected to an external 12MHz crystal oscillator. |
| 11 | 16 | VBAT | PWR | **3.3V~3.6V Battery Power Input (RTC)**<br>An external filtering capacitor must be connected to ensure stable power supply. |
| 53 | 73 | VDD33A | PWR | **3.3V Power Input (LCD)**<br>Near the pin end, an external 10uF and a 0.1uF filtering capacitor must be connected to ground.<br>Note: This power input should be powered independently and should not be directly connected to VDD33_iO or AVDD. |
| 5, 29 | 8, 15, 35 | VDD33B | PWR | **3.3V Power Input (MCU)**<br>This pin requires an external 1uF and 0.1uF filtering capacitor to be connected to ground and ensure stable power supply. |
| 51, 52, 54 | 63, 68, 81 | VDD33_IO1 | PWR | **3.3V Power Input (I/O)**<br>These pins require an external 2.2uF and 0.1uF filtering capacitor to be connected to ground and ensure stable power supply. |
| 81 | 90, 102, 113 | VDD33_IO2 | PWR | **3.3V Power Input (I/O)**<br>These pins must be connected to an external 2.2uF and 0.1uF filtering capacitor to ground, and separated from VDD33_IO1 to ensure stable power supply Please refer to the application circuit in Chapter 9. |
| 23, 89 | 28, 22 | AVDD | PWR | **Power Input of Internal Analog Circuit**<br>Provide 3.3V voltage, and a 1uF and a 0.1uF filtering capacitor must be externally connected to the ground near the pin end. |
| 6 | 9 | VDD12 | PWR | **1.2V Core Power Output (MCU)**<br>Near the pin end, an external 1uF and a 0.1uF filtering capacitor must be connected to ground. |

| Pin # LT7589A | Pin # LT7589B | Pin Name | I/O | Description |
|---|---|---|---|---|
| 55, 71, 90 | 64, 70, 123 | LCD_V12 | PWR | **1.2V Core Power Output (LCD)**<br>Just connect an external 0.01uF filtering capacitor to ground near the pin end.<br>Note: The external capacitor should not exceed 0.01uF and should not be connected to VDD12. |
| 96 | 11, 29, 65, 28 | VSS | PWR | **GND Ground** |
| -- | 82, 91, 103 | VSS_C | PWR | **Core GND Ground** |
| 0 | -- | Thermal Pad | - | **Heat Dissipation Pad**<br>The heat dissipation pads on the back of the LT7589B package must be directly grounded.<br>Note: In order to achieve better soldering results, it is recommended to refer to the instructions in Figure 8-3 when PCB Layout. |

## 6.11 GPIO Resources of Different TFT Panels

**Table 6-11: LT7589A GPIO Resources**

| Chip / Functions | LT7589A (QFN-96) | |
|---|---|---|
| TFT Panel Data | RGB 565 I/F | RGB 888 I/F |
| Resolution(Max.) | 1280x800 (Serial Protocol Mode) | 1280x800 (Serial Protocol Mode) |
| Flash | 2MB | 2MB |
| SRAM | 256KB+512KB | 256KB+512KB |
| Display RAM | 16MB | 16MB |
| USB 2.0 | V (DP/DM) | V (DP/DM) |
| RTC | V | V |
| SCI Communication Port | V (RXD1, TXD1) | V (RXD1, TXD1) |
| Ext. SPI Flash | V (758_SF) | V (758_SF) |
| Back-Light Control | V (758_PWM1) | V (758_PWM1) |
| SWD Programming Port | V (SWD) | V (SWD) |

| TP Type / IO Port | xTP (1) | CTP | RTP (2) | xTP | CTP | RTP |
|---|---|---|---|---|---|---|
| Total Number of IO Ports | 38 | 34 | 33 | 30 | 26 | 25 |
| IO Port Type Description | GPIO (2), GINT, PWM, SCI, QSPI, ADCIN | GPIO (2), GINT, PWM, SCI, QSPI, ADCIN | GPIO (2), GINT, PWM, SCI, QSPI, ADCIN | GINT, PWM, SCI, QSPI, ADCIN | GINT, PWM, SCI, QSPI, ADCIN | GINT, PWM, SCI, QSPI, ADCIN |

**Table 6-12: LT7589B GPIO Resources**

| Chip / Functions | LT7589B (LQFP-128) | |
|---|---|---|
| TFT Panel Data | RGB 565 I/F | RGB 888 I/F |
| Resolution(Max.) | 1280x800 (Serial Protocol Mode) | 1280x800 (Serial Protocol Mode) |
| Flash | 2MB | 2MB |
| SRAM | 256KB+512KB | 256KB+512KB |
| Display RAM | 16MB | 16MB |
| USB 2.0 | V (DP/DM) | V (DP/DM) |
| RTC | V | V |
| SCI Communication Port | V (RXD1, TXD1) | V (RXD1, TXD1) |
| Ext. SPI Flash | V (758_SF) | V (758_SF) |
| Back-Light Control | V (758_PWM1) | V (758_PWM1) |
| SWD Programming Port | V (SWD) | V (SWD) |

| TP Type / IO Port | xTP (1) | CTP | RTP (2) | xTP | CTP | RTP |
|---|---|---|---|---|---|---|
| Total Number of IO Ports | 46 | 42 | 41 | 38 | 34 | 33 |
| IO Port Type Description | GPIO (2), GINT, PWM, SCI, QSPI, ADCIN | GPIO (2), GINT, PWM, SCI, QSPI, ADCIN | GPIO (2), GINT, PWM, SCI, QSPI, ADCIN | GPIO, GINT, PWM, SCI, QSPI, ADCIN | GPIO, GINT, PWM, SCI, QSPI, ADCIN | GPIO, GINT, PWM, SCI, QSPI, ADCIN |

**Notes:**

(1) XTP means without TP

(2) Add 8 GPIO

(3) RTP needs to add an RTP control chip (such as TSC2046)

# 7. Function Description

The LT7589 integrates a high-performance 32-bit MCU and a TFT LCD graphic display controller (hereinafter referred to as the TFT LCD controller). The main architecture of this MCU is the same as that of the LT32U05 from Levetop Semiconductor, with 2Mbytes of Flash program space and 768Kbytes of SRAM. Its functions can be directly referred to in the LT7589 MCU core specification or application manual. Therefore, the functional part of the 32-bit MCU will not be described in detail in this specification. In addition, the TFT LCD graphics accelerator adopts the LT7586 hardware architecture of Levetop Semiconductor, with 128Mbytes of display memory and JPG decoder. Its connection with the 32-bit MCU is shown in the following figure:

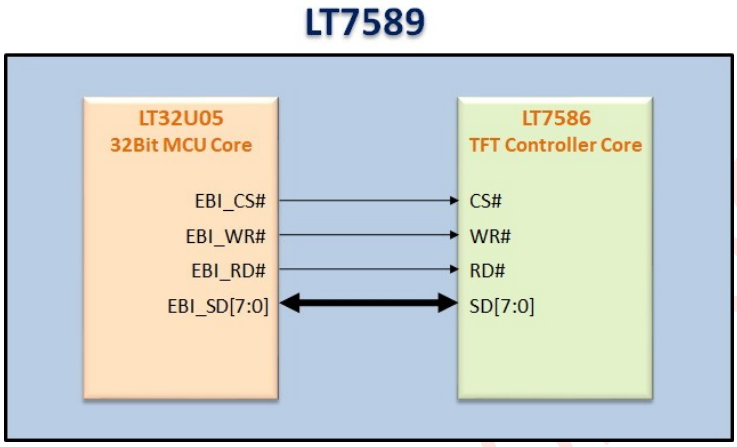



**Figure 7-1: Communication Mode between LT7589 Internal MCU and TFT Graphics Accelerator**

When using LT7589 as a Serial Uart TFT controller, its communication mode with the Host control MCU is through the Uart interface. LT7589 has three sets of SCI (Uart) serial ports, and by default, the second set of TXD1 and RXD1 is used to communicate with the main control MCU. As for the development of the internal MCU program of LT7589, please refer to the LT7589 application manual. Levetop Semiconductor also provides a complete development environment or programming tool.

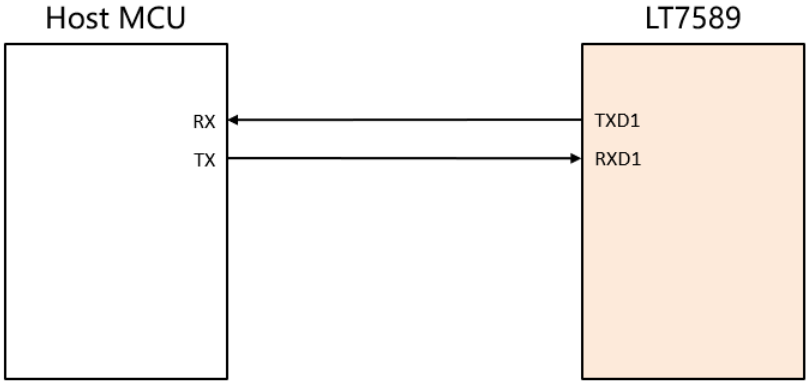



**Figure 7-2: Communication Mode with the Host MCU**

When developing as a serial Uart TFT Controller, the internal MCU program of LT7589 will provide a serial protocol program. Users can use the UI_Editor software provided by Levetop Semiconductor to import the already designed UI structure flow such as images and animations, and complete the development of TFT display. Basically, there is no need to modify the internal MCU program of LT7589, nor do they need to understand the internal registers and control methods of LT7589. The host control MCU program only needs to send the instruction format of the serial protocol according to the product application, and receive and interpret the feedback information sent by LT7589. Therefore, it saves a lot of time in TFT panel display development work.

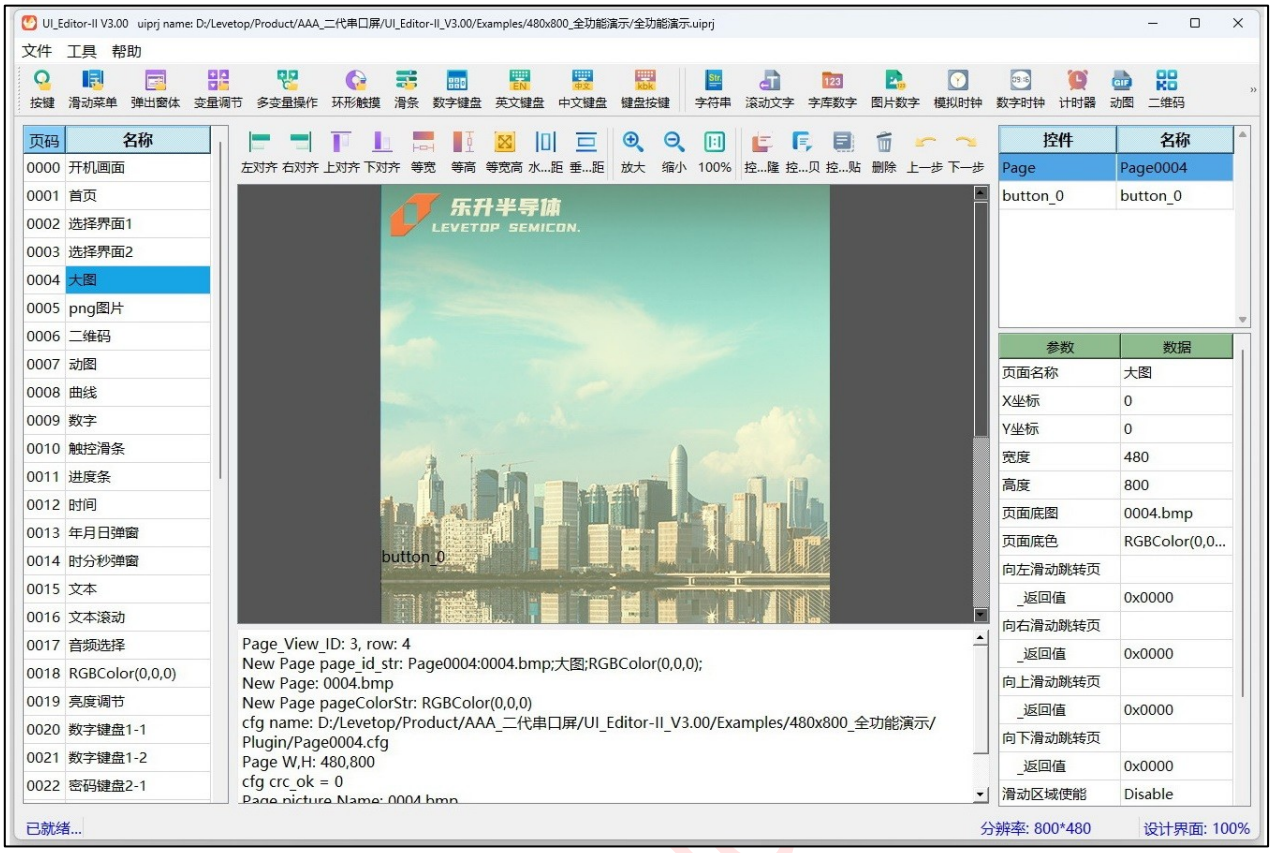



**Figure 7-3: The Main Screen of UI_Editor Tool**

Note: When developing the LT7589 serial Uart TFT Controller, the internal 2Mbytes Flash is used to store the boot program and serial protocol program. During the sample development stage, the samples provided by Levetop Semiconductor will include the boot program, making it convenient for users to update the serial protocol program and develop or modify their own code. During the mass production stage, the chip provided does not include any program (Flash is blank), and users must burn it themselves during production. For code updates and programming, please refer to the LT7589 programming manual.

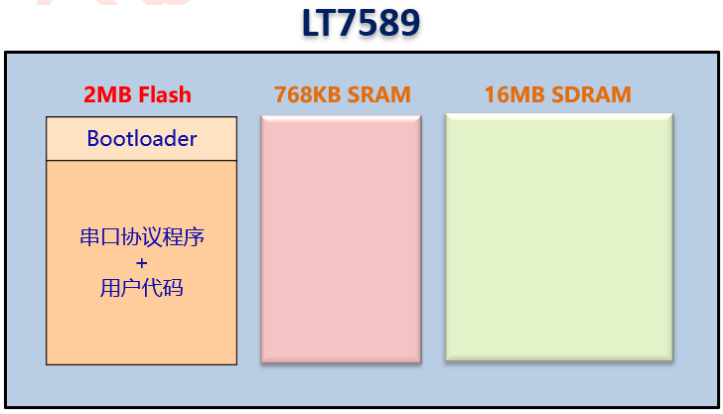



**Figure 7-4: LT7589 Internal Memory**

# 8. Package Information

## 8.1 LT7589A (QFN-96pin)

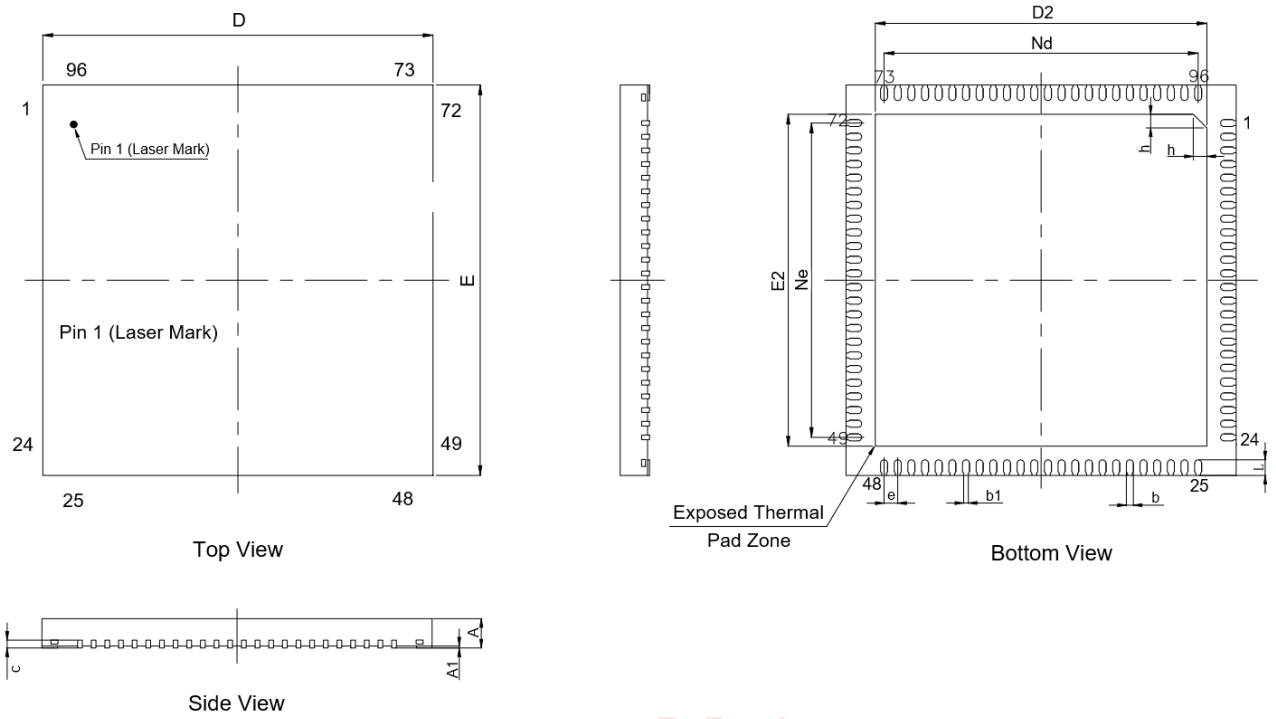



**Figure 8-1: QFN-96Pin Outline**

**Note:** When laying out the PCB, the thermal pad zone on the back of LT7589A must be directly grounded.

**Table 8-1: QFN-96Pin Dimensions**

| Symbol | Millimeter | | | Symbol | Millimeter | | |
|---|---|---|---|---|---|---|---|
| | Min. | Nom. | Max | | Min. | Nom. | Max |
| A | 0.80 | 0.85~1.10 | 1.15 | E | 9.90 | 10.00 | 10.10 |
| A1 | - | 0.02 | 0.05 | Ne | 8.05BSC | | |
| b | 0.13 | 0.18 | 0.23 | L | 0.35 | 0.40 | 0.45 |
| b1 | 0.12REF | | | E2 | 8.40 | 8.50 | 8.60 |
| c | 0.18 | 0.20 | 0.25 | h | 0.30 | 0.35 | 0.40 |
| D | 9.90 | 10.00 | 10.10 | Nd | 8.05BSC | | |
| D2 | 8.40 | 8.50 | 8.60 | | | | |
| e | 0.35BSC | | | | | | |

## 8.2 LT7589B (LQFP-128pin)

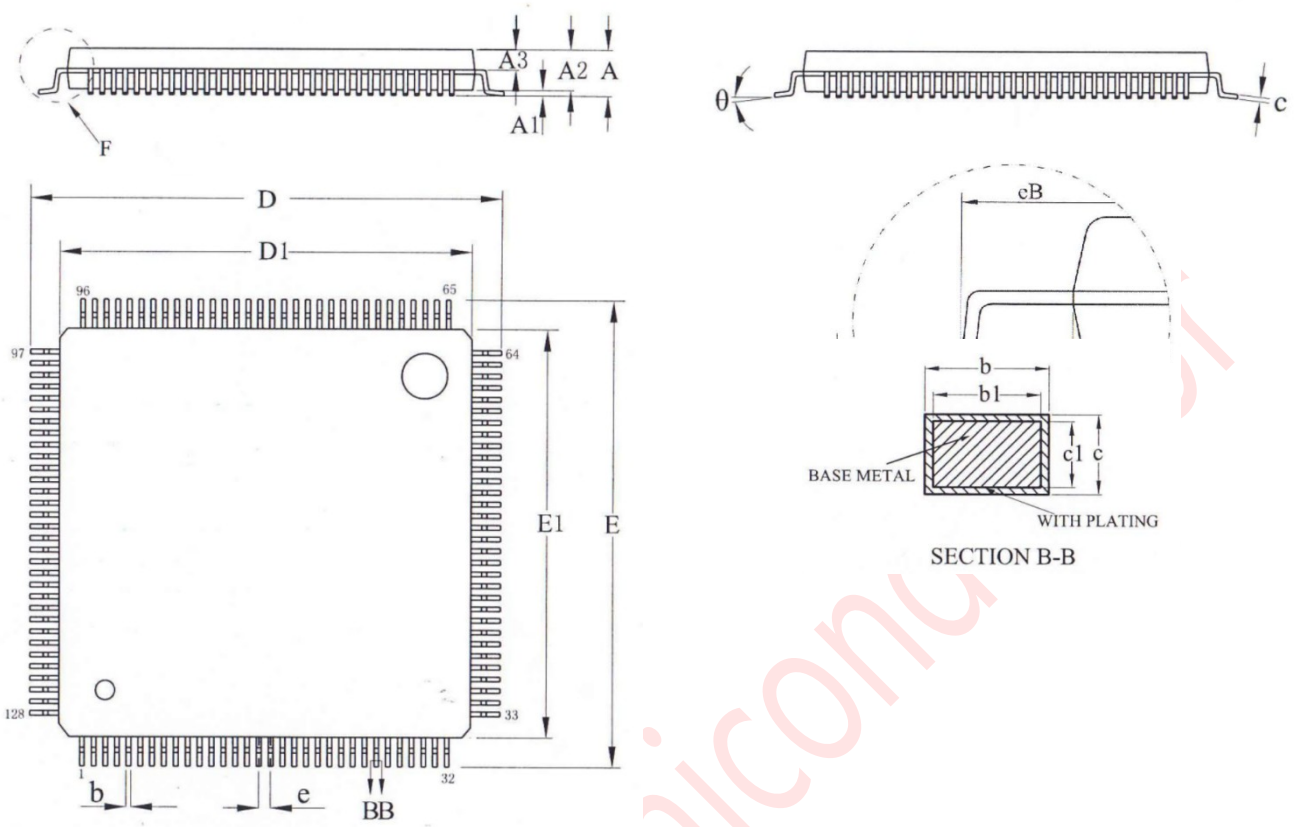



**Figure 8-2: LQFP-128Pin Outline**

**Table 8-2: LQFP-128Pin Dimensions**

| Symbol | Millimeter | | | Symbol | Millimeter | | |
|---|---|---|---|---|---|---|---|
| | Min. | Nom. | Max | | Min. | Nom. | Max |
| **A** | - | - | 1.60 | **D1** | 13.9 | 14.0 | 14.1 |
| **A1** | 0.05 | - | 0.15 | **E** | 15.8 | 16.0 | 16.2 |
| **A2** | 1.35 | 1.40 | 1.45 | **E1** | 13.9 | 14.0 | 14.1 |
| **A3** | 0.59 | 0.64 | 0.69 | **eB** | 15.05 | - | 15.35 |
| **b** | 0.14 | - | 0.22 | **e** | 0.40BSC | | |
| **b1** | 0.13 | 0.16 | 0.19 | **L** | 0.45 | - | 0.75 |
| **c** | 0.13 | - | 0.17 | **L1** | 1.00REF | | |
| **c1** | 0.12 | 0.13 | 0.14 | **θ** | 0 | | 7 |
| **D** | 15.8 | 16.00 | 16.2 | | | | |

## 8.3 LT7589A PCB Layout Suggestions

LT7589A adopts QFN packaging, with ground (GND) heat dissipation pads on the back of the chip. In order to achieve better heat dissipation and reduce soldering risks, it is recommended to divide the PCB copper foil surface of the bottom solder pad of LT7589A into four or more small solder surfaces (square or circular) during PCB layout, and set the interval between each solder surface to~0.8mm to avoid incomplete soldering caused by the use of complete solder surfaces with the same or even larger size than LT7589A solder pads, or chip deformation and poor contact caused by PCB and chip solder pad pulling after solder cooling. The correct PCB pad layout is shown in the following two examples of LT7589A. The light-yellow area in the middle is the grounding pad at the bottom of LT7589A, and the gray area is the PCB grounding small pad (welding surface). Each pad can be grounded 1-2 times through a through-hole.

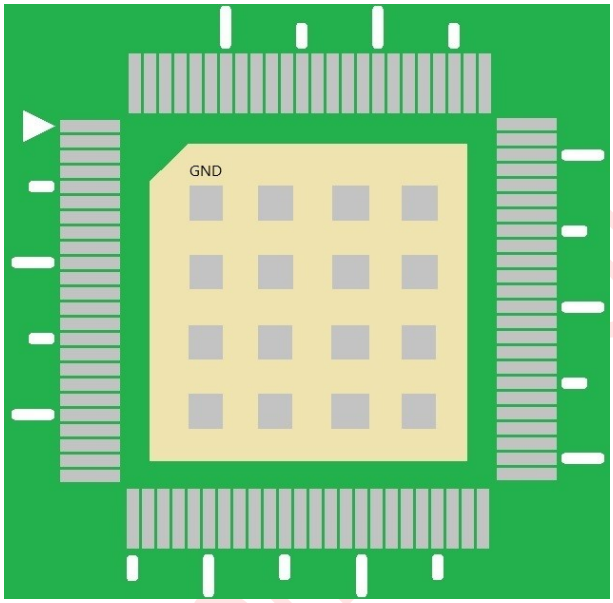



**Figure 8-3: Design Suggestion-1 for LT7589A Bottom Pad PCB Layout**

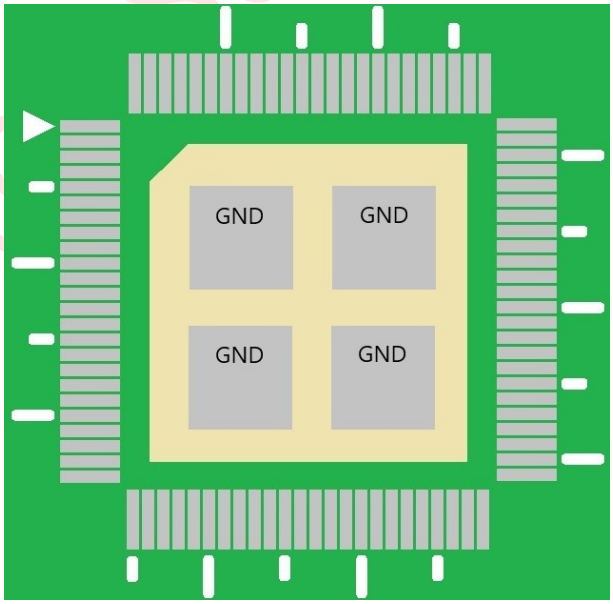



**Figure 8-4: Design Suggestion-2 for LT7589A Bottom Pad PCB Layout**

# 9. Application Circuit

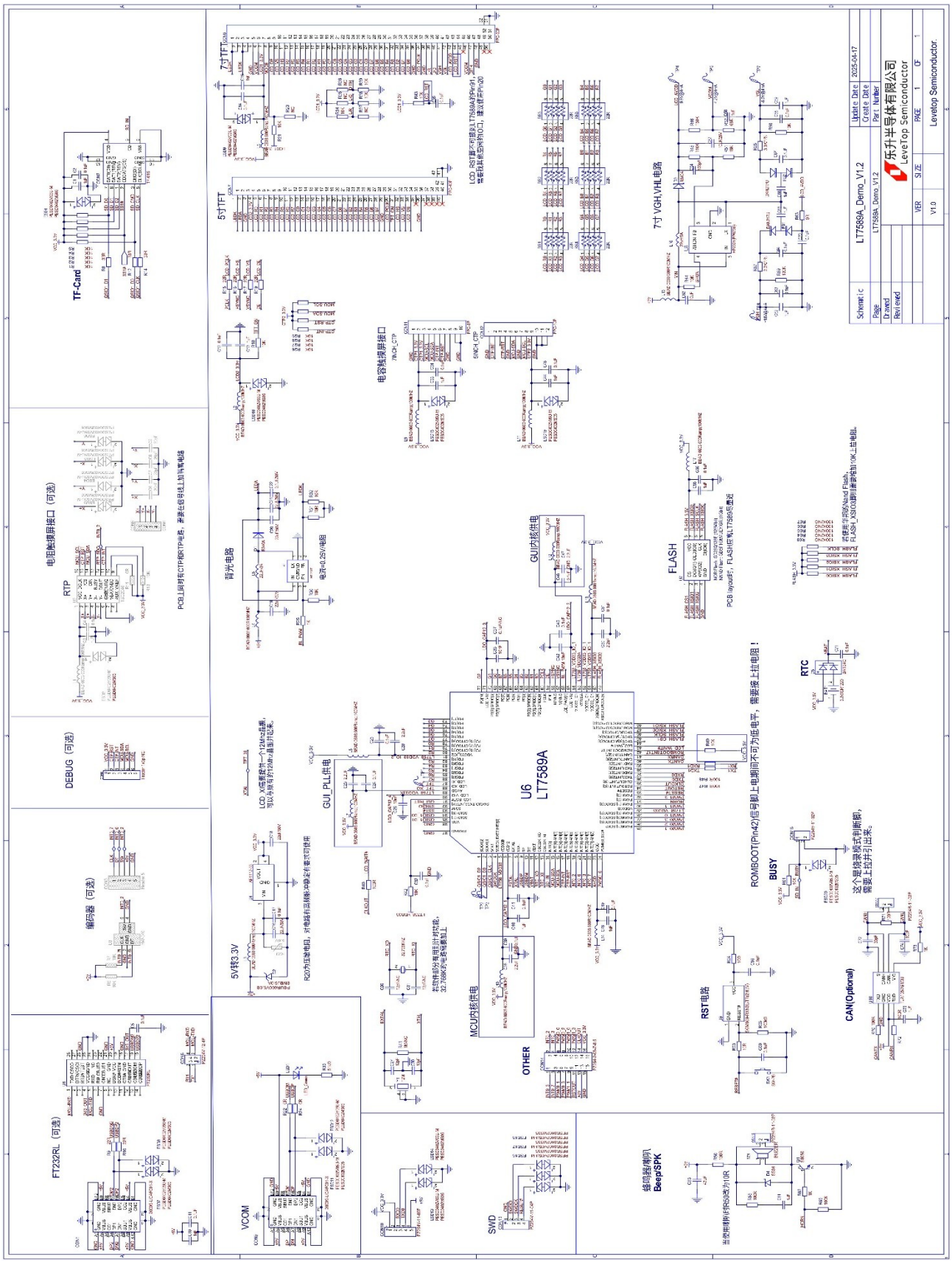



**Figure 9-1: LT7589A Application Circuit**

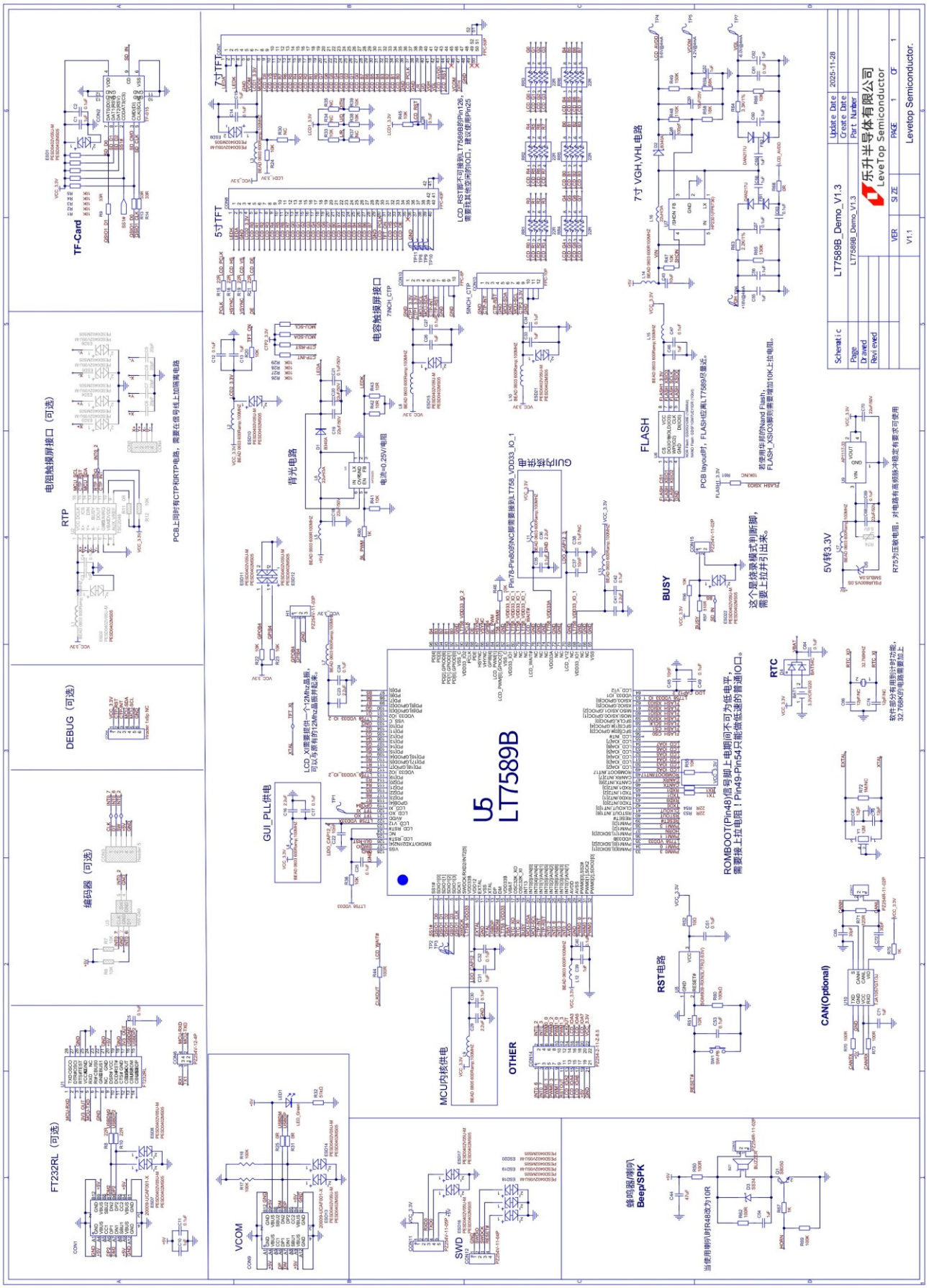



**Figure 9-2: LT7589B Application Circuit**