乐升半导体
LEVETOP

LT7580
LT7586B

TFT-LCD Graphics Display Controller

Brief Specification

V 1.5

www.levetop.cn
Levetop Semiconductor Co., Ltd.

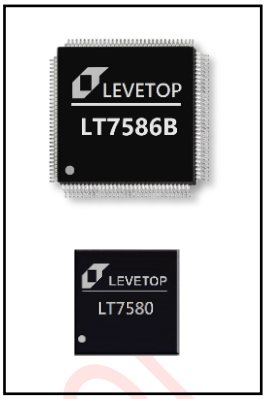
Version History

Version	Date	Description
V1.0	2025/2/18	● First Version.
V1.1	2025/3/20	● Update Application Circuit
V1.2	2026/01/12	● Update Figure 1-4, 1-5, 1-6, 9-1 (LT7586B Schematic) ● Update Table 2-8
V1.2	2026/02/27	● Update LT7583 Information

Copyright

Contents

1. Chip Introduction



LT7586 is a series of high-performance TFT color LCD graphics acceleration display controller, supporting display resolutions from 480*480 to 1280*1024 (SXGA), adapting to various MCU interfaces, and can drive 16bit s (5/6/5) or 24bit s (8/8/8) RGB interface TFT display panels, and achieve Alpha RGB: 8888 color depth. This series includes three chips, namely LT7586 and LT7580, using LQFP-128 and QFN-80 Pin packaging types.

LT7586 provides SPI, I2C serial port and 8/16-bit MCU parallel port interface, built-in 128Mb display memory, supports 65K colors at 16bits per pixel or 16M colors at 24bits per pixel. It comes with JPG hardware decoder and hardware graphics acceleration engine (BTE) to provide command-type graphics operations, such as image mirroring, picture-in-picture (PIP), graphics mixing, transparent display and other functions. It has a built-in geometric drawing engine that supports drawing points, lines, curves, ellipses, triangles, rectangles, rounded rectangles and other functions. It also has a QSPI Master interface, which can be plugged in with 2 high-speed QSPI components such as SPI Flash. Through DMA mode, the UI display material stored in the Flash is extracted to the display memory, and the panel can be displayed directly and quickly without the need to transmit the color image data through the MCU, which reduces the software and hardware operation of the MCU.

The LT7586 provides powerful display performance and industrial-grade specifications, supports long-term supply, and is suitable for electronic products that require TFT color LCD display, such as Smart home appliances, industrial control equipment, car dashboards, motorcycle / battery vehicles / motorized bicycles / scooters / balance vehicles / special vehicle instruments, electronic instruments, medical testing equipment, electronic beauty equipment, water purification equipment, air purifiers, testing equipment, charging piles, energy storage equipment / UPS / inverters, multi-function machines, commercial printers, audio systems, elevator indicators and other products.

1.1 Internal Block Diagram

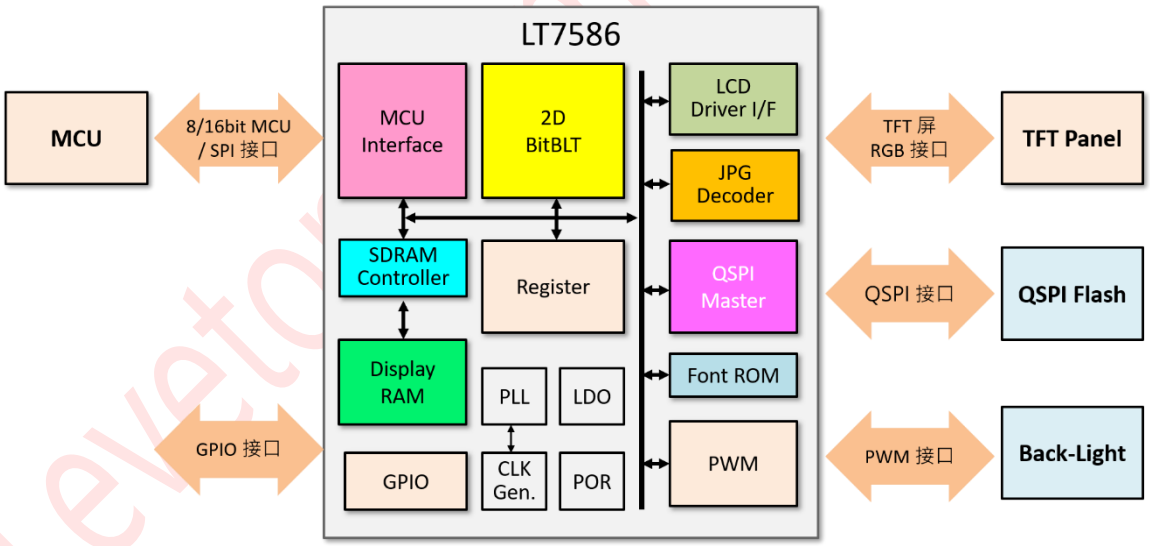


Figure 1-1: LT7586 Internal Block Diagram

1.2 System Application Block Diagram

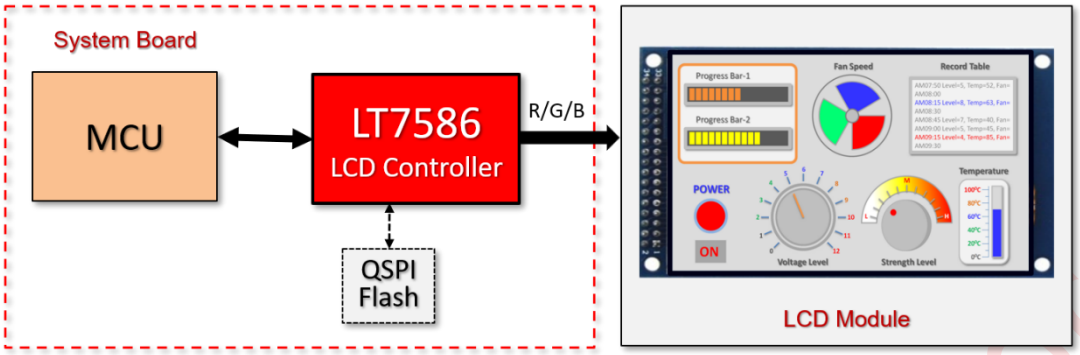


Figure 1-2: LT7586 Setup on System Motherboard

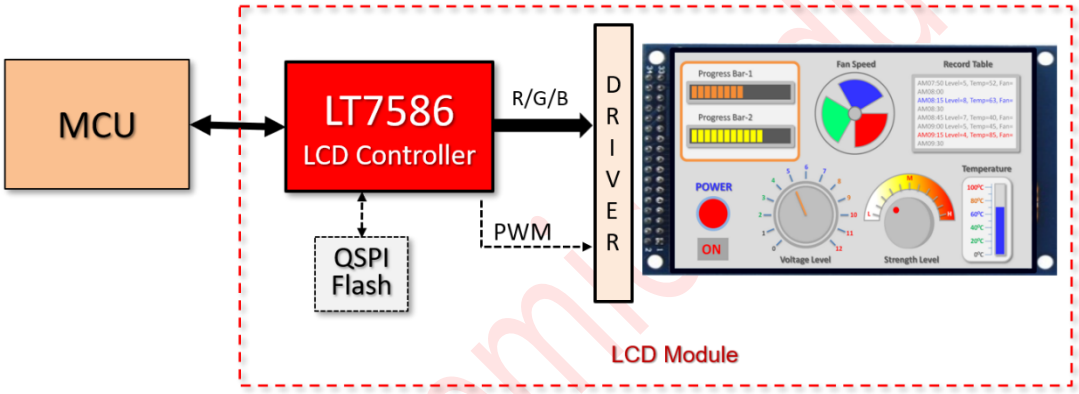


Figure 1-3: LT7586 Installed on LCD Module

1.3 Model Information

Table 1-1: Model Description

Part Number	Package	Embedded Display RAM	Resolution	Color Depth
LT7586B	LQFP-128	128Mbit	1280*1024	16.7M colors
LT7580	QFN-80	128Mbit	1024*768	16.7M colors

1.4 Function Introduction

MCU Interface

- Supports 8-bit or 16-bit 8080 or 6800 parallel ports.
- Supports 3-wire or 4-wire SPI serial interface.
- Support I2C serial interface.

Display Memory

- **Built-in 128Mb Display RAM memory.**

Display Color Data Format

- 16bpp : Color RGB 5:6:5 (2 bytes/pixel).
- 24bpp : Color RGB 8:8:8 (3 bytes/pixel or 4 bytes/pixel).
  - α RGB 4:4:4:4 (4,096 indexed colors / pixel, including transparency attribute)
- **32bpp : Color α RGB 8:8:8:8 (4 bytes/pixel).**

Panel Interface and Resolution

- Support 16 and 24bits RGB interface panels.
- Supported resolutions:
  - WQVGA: 480*480 *16/24bits TFT Panel
  - VGA : 640*480 *16/24bits TFT Panel
  - WVGA : 800*480 *16/24bits TFT Panel
  - SVGA : 800*600 *16/24bits TFT Panel
  - QHD : 960*540 *16/24bits TFT Panel
  - WSVGA: 1024*600 *16/24bits TFT Panel
  - XGA : 1024*768 *16/24bits TFT Panel
  - SXGA : 1280*1024 *16/24bits TFT Panel

Graphic Display Function

- **Built-in JPG hardware decoder**
- Supports users to define 4 32*32 graphic cursors.
- Provides virtual display function: Virtual display can display images larger than the size of the LCD panel so that the image can be easily scrolled in any direction.
- Provides Picture-in-Picture (PIP) display: supports two PIP window areas: the enabled PIP window is displayed on top of the main window, and the PIP1 window is displayed on top of the PIP2 window.
- Supports multiple display functions: the main display window can be switched between display buffers to achieve simple animation display effects.
- Supports the function of quickly displaying images upon wakeup.
- Supports mirroring and vertical flip display functions.
- Color Bar Display: It can still be displayed in a color bar format without writing data to the internal display memory. The default resolution is 640*480 pixels.

Block Transfer Engine (BitBLT)

- Built-in 2D BitBLT engine.
- Provides copy image functionality with raster operations.
- Provides color depth conversion.
- Solid fill and pattern fill functions:
  - Provides user-defined 8*8 image or 16*16 image.
- Provides the function of synthesizing two images into one image:
  - Chroma-Keying: Blends an image with a specified RGB color based on transparency
  - Graphics blending transparency mode (Window Alpha-Blending): Blends two images based on the transparency within the specified area.
  - Dot Alpha-Blending: Blends two images based on RGB format and transparency.

Geometry Accelerator

- Provides drawing functions such as drawing points, lines, curves, ellipses, triangles, rectangles, and rounded rectangles.

Text Display Function

- Built-in 8*16, 12*24, 16*32 fonts of ISO/IEC 8859-1/2/4/5.
- Supports user-defined half-size and full-size fonts (8*16, 12*24, 16*32).
- Provides a programmable text cursor.
- Supports vertical and horizontal enlargement of fonts (*1, *2, *3, *4 times).
- Support 90-degree rotation of text.

QSPI Master Interface

- Supports copying external serial flash data to the frame buffer.
- **Compatible with standard QSPI specifications (NOR/NAND Flash).**
- Provides 16-byte read FIFO and 16-byte write FIFO.
- An interrupt is issued when the Tx FIFO is completely empty and the SPI Tx/Rx engine is idle.
- **Supports Nand Flash bad block processing.**
- **Support MCU to SPI Flash by Pass Mode.**

I2C Interface

- Provides an I2C interface to connect to external I2C devices.
- Provides standard transmission mode (100kbps) and fast transmission mode (400kbps).

PWM Interface

- Built-in 2 sets of 16-bit counters.
- Programmable duty cycle.

GPIO Interface

- Provides up to 28 GPIO interfaces.

Clock

- Built-in programmable PLL to provide internal clock, external LCD clock, and internal display memory clock.

Power Saving Mode

- Provides three power saving modes: Standby, Suspend and Sleep.
- Supports MCU software and external interrupt wake-up.

Reset Method

- Provide power-on reset, external hardware reset and software command reset.

Power Supply

- VDD voltage: 3.3V +/- 0.3V.
- Built-in 1.2V LDO.

Package Type

- LQFP-128Pin package.
- QFN-80Pin package.

Operating Temperature

- -40℃ ~85℃.

1.5 Chip Pinout

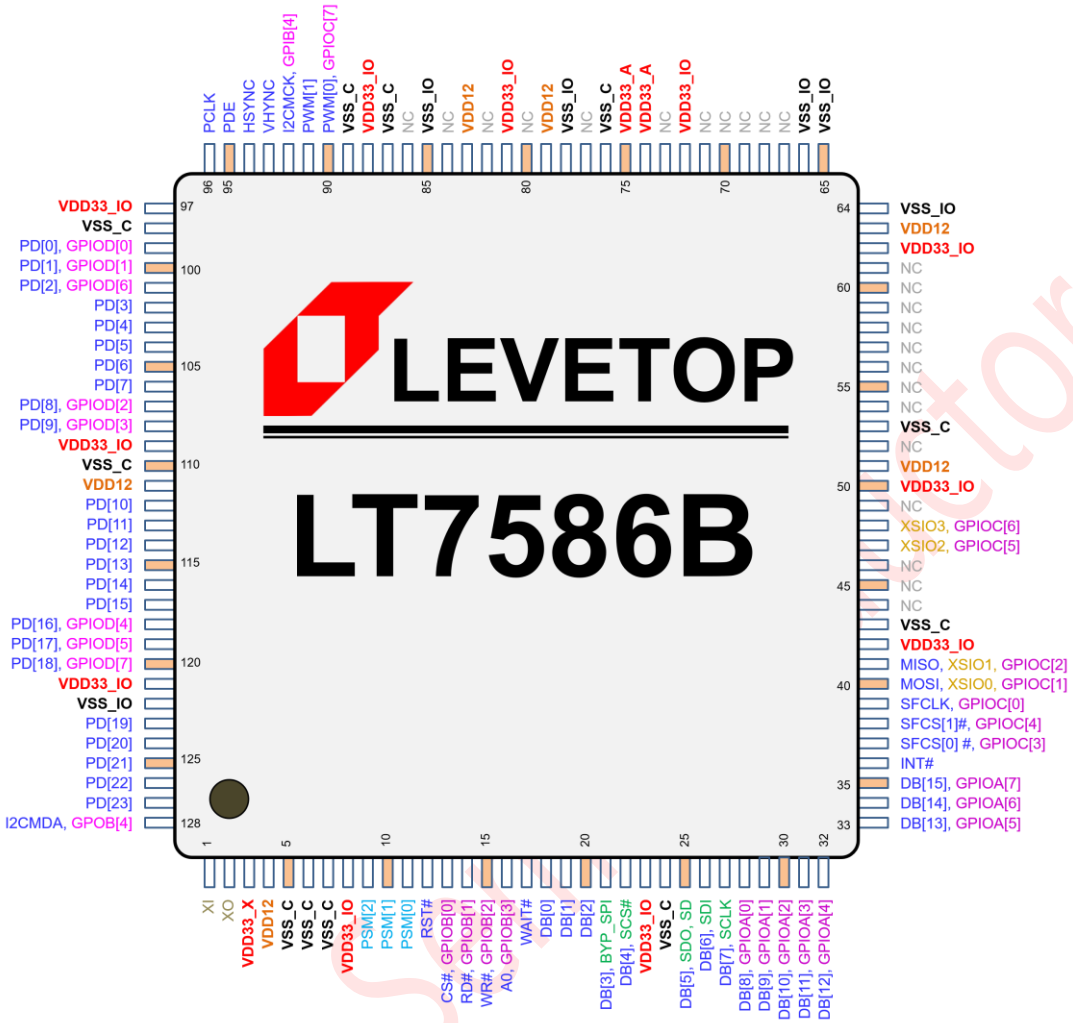


Figure 1-4: LT7586B Pin Diagram (LQFP-128Pin)

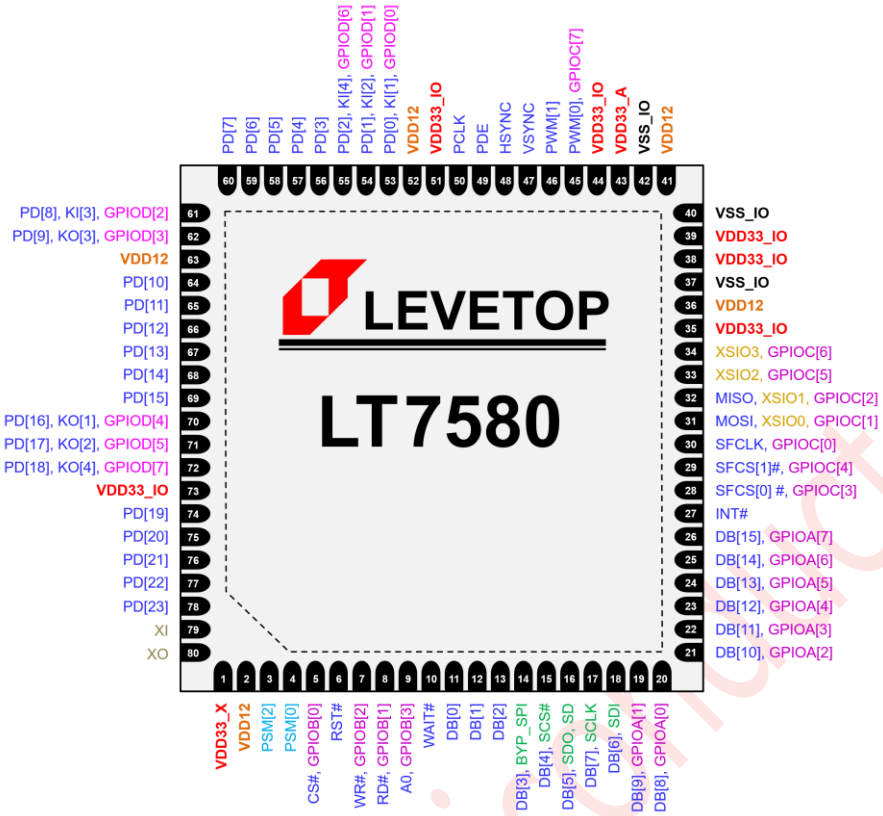


Figure 1-5: LT7580 Pin Diagram (QFN-80 Pin)

2. Pin Signal Description

2.1 MCU Interface Setting Signal

Table 2-1: MCU Interface Setting Signals

<table>
<tr><th>LT7586B Pin#</th><th>LT7580 Pin#</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>9
10
11</td><td>3
--
4</td><td>PSM[2]
PSM[1]
PSM[0]</td><td>I</td><td>MCU Interface Settings
<table>
<tr><th>PSM[2:0]</th><th>MCU Connection Mode</th></tr>
<tr><td>0 0 X</td><td>Select parallel port 8-bit or 16-bit 8080 mode</td></tr>
<tr><td>0 1 X</td><td>Select parallel port 8-bit or 16-bit 6800 mode</td></tr>
<tr><td>1 0 0</td><td>Select the serial port 3-wire SPI mode</td></tr>
<tr><td>1 0 1</td><td>Select the serial port 4-wire SPI mode (supports By-Pass mode)</td></tr>
<tr><td>1 1 0</td><td>Select serial port I2C mode (continuous reading mode is not supported)</td></tr>
<tr><td>1 1 1</td><td>Select serial port I2C mode (support continuous reading mode)</td></tr>
</table>
If the MCU interface is set to parallel mode, PSM[0] is the external interrupt input pin.

The PSM[1] of LT7580 is directly grounded internally and only supports 8-bit or 16-bit 8080 parallel port mode or 3-wire or 4-wire SPI mode.</td></tr>
</table>

2.2 MCU parallel port Signals

Table 2-2: MCU Parallel Port Signals

<table>
<tr><th>LT7586B Pin#</th><th>LT7580 Pin#</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>35~25,
22~18</td><td>26 ~ 11</td><td>DB[15:0]</td><td>IO</td><td>MCU Data Bus

When the interface connecting to the MCU is set to parallel port mode, these data buses serve as the data transmission interface with the MCU.

DB[15:8] can be set to be used as a GPIO interface in 8-bit parallel port mode.

DB[7:0] is also a shared pin. If set to serial port mode, these data buses will be used as serial port signals. Please refer to Table 2-1 "MCU Interface" for description.</td></tr>
<tr><td>13</td><td>5</td><td>CS#
GPIOB[0]</td><td>I
PU</td><td>Chip Select Signal

CS# = 0, indicating that the MCU is executing a command or data read/write cycle on the LT7586.

If the MCU interface is set to serial port mode, this pin can be set to GPIOB[0] with an internal pull-up resistor.</td></tr>
</table>

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
14	8	RD# EN GPIOB[1]	I PU	**Read Control Signal** In 8080 parallel port mode, this pin is the RD# signal, RD# = 0, indicating that the MCU is performing a data read or status read cycle on the LT7586. In 6800 parallel port mode, this pin is the EN signal, EN = 1, indicating that the MCU's control over the LT7586 is in the enable cycle. If the MCU interface is set to serial port mode, this pin can be set to GPIOB[1] with an internal pull-up resistor.
15	7	WR# RW# GPIOB[2]	I PU	**Write Control Signal** In 8080 parallel port mode, this pin is the WR# signal. WR# = 0 means that the MCU is writing commands or data to the LT7586. In 6800 parallel port mode, this pin is the RW# signal. RW# = 1 means that the MCU is performing a data read or status read cycle on the LT7586. RW# = 0 means that the MCU is performing a command write or data write cycle on the LT7586. If the MCU interface is set to serial port mode, this pin can be set to GPIOB[2] with an internal pull-up resistor.
16	9	A0 GPIOB[3]	I	**Command Or Data Selection Signal** A0 = 0, indicating that the MCU performs a status read or command write cycle on the LT7586. A0 = 1, indicating that the MCU is performing a data read or data write cycle on the LT7586. If the MCU interface is set to serial port mode, this pin can be set to GPIOB[3] with an internal pull-up resistor.
36	27	INT#	O	**Interrupt Output Signal** When the set interrupt condition occurs, this pin becomes low level to generate an interrupt output to inform the MCU.
17	10	WAIT#	O	**Wait Signal** When MCU reads and writes LT7586, if LT7586 is in a busy state, WAIT# will become a low level to inform MCU to enter the waiting cycle.

2.3 MCU Serial Port Signals

Table 2-3: MCU Serial Port Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
27	17	SCLK (DB[7])	I	**Serial Port Clock Signal** When the interface connected to the MCU is set to serial port mode (SPI or I2C), this pin is the serial port clock signal. This is a pin shared with the parallel port data line DB[7].
26	18	SDI I2C_SD (DB[6])	I	**4-Wire SPI Data Input; I2C Data Signal** In the serial port 4-wire SPI mode, SDI represents the serial port data input, which is to receive the MOSI output signal from the MCU. In serial I2C mode, I2C_SD represents the I2C data pin. This pin is not used in 3-wire SPI mode, please connect it to ground (GND).
25	16	SDO SD I2CA[5] (DB[5])	IO	**4-Wire SPI Data Output; 3-Wire SPI Data Signal; I2C Address Selection Signal** In the serial port 4-wire SPI mode, SDO represents the serial port data output to the MISO input terminal of the MCU. In the serial port 3-wire SPI mode, SD represents the bidirectional data pin of the 3-wire SPI. In serial I2C mode, this pin is the I2C device address bit[5]. This is a pin shared with the parallel port data line DB[5].
22	15	SCS# I2CA[4] (DB[4])	I	**SPI Chip Select Signal; I2C Address Select Signal** In serial port SPI mode, SCS# represents the SPI chip select signal. In serial I2C mode, this pin is the I2C device address bit[4]. This is a pin shared with the parallel port data line DB[4].
21	14	BYP_SPI I2CA[3] (DB[3])	I	**By-Pass MCU-SPI Control Signal** It has the highest priority. When set to high voltage in 4-wire SPI mode, the MCU-SPI signal group will be determined by the value pre-written in register 0xB7[7] and the SPI-Master input and output of SFCS[0]# or SFCS[1]#. In serial I2C mode, this pin is the I2C device address bit[3]. It shared with the parallel port data line DB[3]. It is not used in 3-wire SPI mode and should be connected to ground (GND).
20 ~18	13 ~11	I2CA[2:0] (DB[2:0])	I	**I2C Address Select Signal** In serial I2C mode, these pins are the I2C device address bits[2:0]. These are pins shared with the parallel port data lines DB[2:0]. They are not used in 3-wire SPI mode, please connect to ground (GND).

2.4 External Serial Flash / SPI Master Signals

Table 2-4: External Serial Flash / SPI Master Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
37	28	SFCS[0]# GPIOC[3]	IO	**External Serial Flash#0 or SPI #0 Chip Select Signal** If the serial SPI function is disabled, this pin can be set to GPIOC[3], which defaults to input function.
38	29	SFCS[1]# GPIOC[4]	IO	**External Serial Flash #1 or SPI #1 Chip Select Signal** If the serial SPI function is disabled, this pin can be set to GPIOC[4], which defaults to input function.
39	30	SFCLK GPIOC[0]	IO	**External SPI Serial Clock Signal** This pin is the serial clock signal output and is connected to an external Serial Flash or SPI device. If the serial SPI function is disabled, this pin can be set to GPIOC[0], which defaults to input function.
40	31	MOSI XSIO0 GPIOC[1]	IO	**SPI Data Output Signal / Master Output Slave Input (MOSI)** LT7586 outputs data to external Serial Flash or SPI components. Single Mode: Data input of SPI Flash or SPI component. For LT7586, it is output. Dual Mode: Use the signal as bidirectional data #0 (XSIO0). Only valid in serial SPI Flash DMA mode. If the serial SPI function is disabled, this pin can be set to GPIOC[1], which defaults to input function.
41	32	MISO XSIO1 GPIOC[2]	IO	**SPI Data Input Signal / Master Input Slave Output (MISO)** LT7586 reads data from external Serial Flash or SPI components. Single Mode: Data output of SPI Flash or SPI component. For LT7586, it is input. Dual Mode: Use the signal as bidirectional data #1 (XSIO1). Only valid in serial SPI Flash DMA mode. If the serial SPI function is disabled, this pin can be set to GPIOC[2], which defaults to input function.
47	33	XSIO2 GPIOC[5]	IO	**Quad SPI Mode, XSIO2 (#WP)** Dual Mode: Use the signal as bidirectional data #2 (XSIO 2). Only valid in Serial SPI Flash DMA mode. If the serial SPI function is disabled, this pin can be set to GPIOC[5], which defaults to input function.

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
48	34	XSIO3 GPIOC[6]	IO	**Quad SPI Mode, XSIO3 (#HOLD)** Dual Mode: Use the signal as bidirectional data #3 (XSIO 3). Only valid in Serial SPI Flash DMA mode. If the serial SPI function is disabled, this pin can be set to GPIOC[6], which defaults to input function.

Note: These external serial Flash signals all run at high speed, and the SPI Flash component must be placed as close to the LT758 as possible when connecting on the PCB.

2.5 PWM Signals

Table 2-5: PWM Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
90	45	PWM[0] GPIOC[7] CCLK	IO	**PWM #0 Output Signal** This is a programmable PWM output signal that can be used to control the backlight of a TFT Panel or other components. The PWM output mode can be set via registers. This pin is shared with GPIOC[7]. If PWM is disabled, the default function of GPIOC[7] is input or output system clock signal (CCLK).
91	46	PWM[1]	IO	**PWM #1 Output Signal** This is a programmable PWM output signal that can be used to control the backlight of a TFT Panel or other components. The PWM output mode can be set via registers.

2.6 LCD Panel Interface Signals

Table 2-6: LCD Panel Interface Signals

<table>
<tr><th>LT7586B Pin#</th><th>LT7580 Pin#</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>127~123,
120~112,
108~99</td><td>78~74,
72~64,
62~53</td><td>PD[23:0]</td><td>IO</td><td>
LCD Data Bus
Outputs RGB data to the TFT-LCD panel, and can be set to connect to the corresponding RGB bus through the register.
<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">TFT-LCD RGB Interface</th></tr>
<tr><th>11b (GPIO)</th><th>10b (16 bits)</th><th>00b (24 bits)</th></tr>
<tr><td>PD[0]</td><td colspan="2">GPIOD[0]</td><td>B0</td></tr>
<tr><td>PD[1]</td><td colspan="2">GPIOD[1]</td><td>B1</td></tr>
<tr><td>PD[2]</td><td colspan="2">GPIOD[6]</td><td>B2</td></tr>
<tr><td>PD[3]</td><td>GPIOE[0]</td><td>B0</td><td>B3</td></tr>
<tr><td>PD[4]</td><td>GPIOE[1]</td><td>B1</td><td>B4</td></tr>
<tr><td>PD[5]</td><td>GPIOE[2]</td><td>B2</td><td>B5</td></tr>
<tr><td>PD[6]</td><td>GPIOE[3]</td><td>B3</td><td>B6</td></tr>
<tr><td>PD[7]</td><td>GPIOE[4]</td><td>B4</td><td>B7</td></tr>
<tr><td>PD[8]</td><td colspan="2">GPIOD[2]</td><td>G0</td></tr>
<tr><td>PD[9]</td><td colspan="2">GPIOD[3]</td><td>G1</td></tr>
<tr><td>PD[10]</td><td>GPIOE[5]</td><td>G0</td><td>G2</td></tr>
<tr><td>PD[11]</td><td>GPIOE[6]</td><td>G1</td><td>G3</td></tr>
<tr><td>PD[12]</td><td>GPIOE[7]</td><td>G2</td><td>G4</td></tr>
<tr><td>PD[13]</td><td>GPIOF[0]</td><td>G3</td><td>G5</td></tr>
<tr><td>PD[14]</td><td>GPIOF[1]</td><td>G4</td><td>G6</td></tr>
<tr><td>PD[15]</td><td>GPIOF[2]</td><td>G5</td><td>G7</td></tr>
<tr><td>PD[16]</td><td colspan="2">GPIOD[4]</td><td>R0</td></tr>
<tr><td>PD[17]</td><td colspan="2">GPIOD[5]</td><td>R1</td></tr>
<tr><td>PD[18]</td><td colspan="2">GPIOD[7]</td><td>R2</td></tr>
<tr><td>PD[19]</td><td>GPIOF[3]</td><td>R0</td><td>R3</td></tr>
<tr><td>PD[20]</td><td>GPIOF[4]</td><td>R1</td><td>R4</td></tr>
<tr><td>PD[21]</td><td>GPIOF[5]</td><td>R2</td><td>R5</td></tr>
<tr><td>PD[22]</td><td>GPIOF[6]</td><td>R3</td><td>R6</td></tr>
<tr><td>PD[23]</td><td>GPIOF[7]</td><td>R4</td><td>R7</td></tr>
</table>
Part of the LCD data bus is shared with GPIO pins. For example, if the LCD is set to 16 bpp function mode, PD[18:16; 9:8; 2:0] is defined as GPIO pins.
</td></tr>
</table>

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
96	50	PCLK	O	**LCD Pixel Clock Signal** The pixel clock signal is connected to the general TFT drive interface signal. This signal is generated by the internal PPLL driver.
93	47	VSYNC LVDS_PD#	O	**LCD Vertical Sync Signal** The vertical synchronization signal VSYNC is connected to a common TFT driving interface signal. When EXT_FLAT_NK (REG[00h] bit1) is set to 1, it will be forced to DE mode, and the VSYNC signal will become LVDS_PD#.
94	48	HSYNC LVDS_PD	O	**LCD Horizontal Sync Signal** The horizontal synchronization signal HSYNC is connected to the general TFT drive interface signal. When Ext_FlatInk (REG[00h] bit1) is set to 1, it will be forced to DE mode, and the HSYNC signal will become LVDS_PD.
95	49	PDE	O	**LCD Panel Data Enable** This signal is the data valid or data enable signal connected to the general TFT drive interface.

2.7 I2C Master Signals

Table 2-7: I2C Master Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
92	--	I2CMCK	I	**I2C Master Clock Signal** This pin is the I2C Master clock signal I2CMCK.
128	--	I2CMDA	O	**I2C Master Data Signal** This pin is the data signal I2CMDA of the I2C Master and is in Open-Drain output mode.

2.8 GPIO Signals

Table 2-8: GPIO Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
35~28	26~19	GPIOA[7:0]	IO	**GPIO Output / Input Signal** GPIOA[7:0] is a general-purpose I/O pin. These pins are shared with DB[15:8]. GPIOA can only be used when the MCU is set to 8 -bit parallel mode or serial mode. The output mode of these pins can be set via registers.

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
92, 128, 16~13	-- -- 9, 7, 8, 5	GPIB[4], GPOB[4], GPIOB[3:0]	IO	**GPIO Output / Input Signal** GPIB[4] shares the pin with I2CMCK; The output data of GPOB[4] shares the pin with I2CMDA; The input signal of GPIOB[3:0] shares the pin with {A0, WR#, RD#, CS#}. When the MCU is set to serial port mode, the output and input modes of these pins can be set through registers.
90, 48, 47, 38, 37, 41, 40, 39	45, 34, 33, 29, 28, 32, 31, 30	GPIOC[7], GPIOC[6:5], GPIOC[4:0]	IO	**GPIO Output / Input Signal** The output data of GPIOC[7] shares the pin with PWM[0]. The GPIOC[7] function can only be used when the PWM function is disabled. GPIOC[6:0] shares pins with {XSIO3, XSIO2, SFCS[1]#, SFCS[0]#, MISO, MOSI, SFCLK} and can only be used when the SPI Master function is disabled. The output modes of these pins can be set via registers.
120, 101 119, 118 108, 107 100, 99	72, 55, 71, 70, 62, 61, 54, 53	GPIOD[7:0]	IO	**GPIO Output / Input Signal** GPIOD[7:0] and PD[18, 2, 17, 16, 9, 8, 1, 0] share pins and can only be used when the LCD panel data bus is set to 16 bits. The output mode of these pins can be set via registers.

2.9 Reset and Test Signals

Table 2-9: Reset and Test Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
12	6	RST#	I/O PU	**Reset Input Signal** When RST# = 0 and remains longer than 32 clock cycles, the LT7586 will generate a reset action.

Note: PU: Pull-up with pull-up resistor; PD: Pull-Down with pull-down resistor; NP: No Pull without pull-up resistor

2.10 Power and Clock Signals

Table 2-10: Power and Clock Signals

LT7586B Pin#	LT7580 Pin#	Pin Name	I/O	Description
1	79	XI	I	**Crystal Oscillator (Crystal) / Clock Signal Input** This pin is connected to an external crystal oscillator and is the input signal for the internal crystal oscillator circuit. When using an active crystal oscillator or an external clock signal, this pin can be used to input the crystal oscillator frequency (OSC) between 5MHz and 30MHz. A 12MHz crystal oscillator is recommended.
2	80	XO	O	**Crystal Output** This pin is connected to an external crystal oscillator and is the output signal of the internal crystal oscillator circuit.
4, 51, 63, 79, 83, 111	2, 36, 41, 52, 63	VDD12	PWR	**Internal LDO 1.2V Power Output** Each VDD12 pin must be connected to a 0.01uF filter capacitor to ground.
3	1	VDD33_X	PWR	**Internal Crystal Oscillator 3.3V Power Input** This VDD33_X pin must be connected to a 0.1uF filter capacitor to ground.
74, 75	43	VDD33_A	PWR	**Internal LDO 3.3V Power Input** The VDD33_A pin must be connected to a 1uF and a 0.1uF filter capacitor to ground, and cannot be directly connected to VDD33_IO. It needs to be isolated with a bead or powered independently.
8, 23, 42, 50, 62, 72, 81, 88, 97, 109, 121	35, 38, 39, 44, 51, 73	VDD33_IO	PWR	**3.3V I/O Power Input** Each VDD33_IO pin must be connected to a 1uF and a 0.1uF filter capacitor to ground.
5, 6, 7, 24, 43, 53, 76, 87, 89, 98, 110	81 (1)	VSS_C	PWR	**Core Power Ground**
64, 65, 66, 78, 85, 122	37, 40, 42	VSS_IO	PWR	**I/O Power Ground** These pins must be tied directly together to VSS_C.

Note (1): This is also the thermal pad zone of the LT7580 and must be connected to VSS or GND.

3. Electrical Characteristics

3.1 Electrical Limit Parameters

Table 3-1: Electrical Limit Parameters

Symbol Name	Parameter's Description	Range	Unit
V_{DD}	Supply Voltage	-0.3 ~ 4.0	V
V_{IN}	Logic Input Voltage	-0.3 ~ VDD+0.3	V
V_{OUT}	Logic Output Voltage	-0.3 ~ VDD+0.3	V
P_D	Maximum Power Consumption	≦ 500	mW
T_{OPR}	Operating Temperature Range	-40 ~ 85	℃
T_{ST}	Storage Temperature Range	-45 ~ 125	℃
T_{SOL}	Maximum Soldering Temperature	260	℃

Note: The maximum limit value means that the chip may be damaged when it exceeds the working range. The recommended working range means that the device functions normally within this range, but it is not completely guaranteed to meet individual performance indicators. The electrical parameters define the DC and AC parameter specifications of the device within the working range and under test conditions that guarantee specific performance indicators. For parameters without upper and lower limits, this specification does not guarantee their accuracy, but their typical values reasonably reflect the performance of the device.

3.2 Electrical Parameters

Conditions: VDD33_A = 3.3V, TA = 25℃, using 800x480 TFT Panel, 8-bit 8080 MCU parallel port - 16bbp test.

Table 3-2: Electrical Parameters

Symbol Name	Parameter's Description	Condition	Min.	Typ.	Max.	Unit
V_{DD33_A}, V_{DD33_IO}	Operating Voltage		3.0	3.3	3.6	V
C_{VDD}	Load Capacitance		1	-	10	uF
I_{OPR}	Working Current	As above		50		mA
I_{STB}	Standby Current	As above		15		mA
I_{SUSP}	Suspend Current	As above		12		mA
I_{SLP}	Sleep Current	As above		5		mA
T_{RMP}	Power Supply Rise Time	VDD Ramp Up to 3.3 V	3.5		35	ms
Oscillator Clock and PLL						
F_{OSC}	Crystal Oscillator (OSC) Frequency	VDD = 3.3V	3.5	1 2	35	MHz
F_{VCO}	VCO Output Frequency		200		400	MHz
T_{LOCK}	Lock Time				50	us
CLK_{MPLL}	MPLL Output Frequency (MCLK)	As above	25	133	180	MHz
CLK_{CPLL}	CPLL Output Frequency (CCLK)	As above	25	1 33	170	MHz
CLK_{PPLL}	PPLL Output Frequency (PCLK)	As above	12.5	3 0	100	MHz

3.3 ESD Protection Specifications

Table 3-3: ESD Protection Specifications

ESD Items	Symbol	Maximum	Unit	Reference Standards
Human Body Model	HBM	4,000	V	ANSI/ESDA/JEDEC JS-001-2017
Machine Model	MM	200	V	JEDEC JESD22-A115C-2010
Charged Device Model	CDM	800	V	ANSI/ESDA/JEDEC JS-002-2022
Latch Up	LU	200	mA	JEDEC JESD78F.01-2022, @105℃

Note: When performing manual welding, it is recommended that personnel and equipment be treated with anti-static measures, such as appropriate temperature and humidity environment, welding equipment grounding, anti-static workbench, and welders wearing anti-static wrist straps, etc.

4. Clock Signal

LT7586 contains a crystal oscillator circuit, which is provided by an external crystal oscillator as the oscillation clock source. It is recommended to use a 12MHz crystal oscillator. The built-in PLL circuit then generates the required clock signal. LT7586 has three built-in PLL circuits according to the needs of internal functions, providing three groups of clock signals:

- **CPLL** : Generates **CCLK** (Core Clock) for use by the MCU interface, BTE engine, graphics engine, and text DMA engine. If a 12MHz crystal oscillator is used, the preset frequency is 96MHz.
- **MPLL** : Generates **MCLK** (Memory Clock) for use by internal display memory, the default frequency is 96MHz.
- **PPLL** : Generates **PCLK** (Pixel Clock) to provide LCD panel's pixel scanning operating frequency, preset 36MHz.

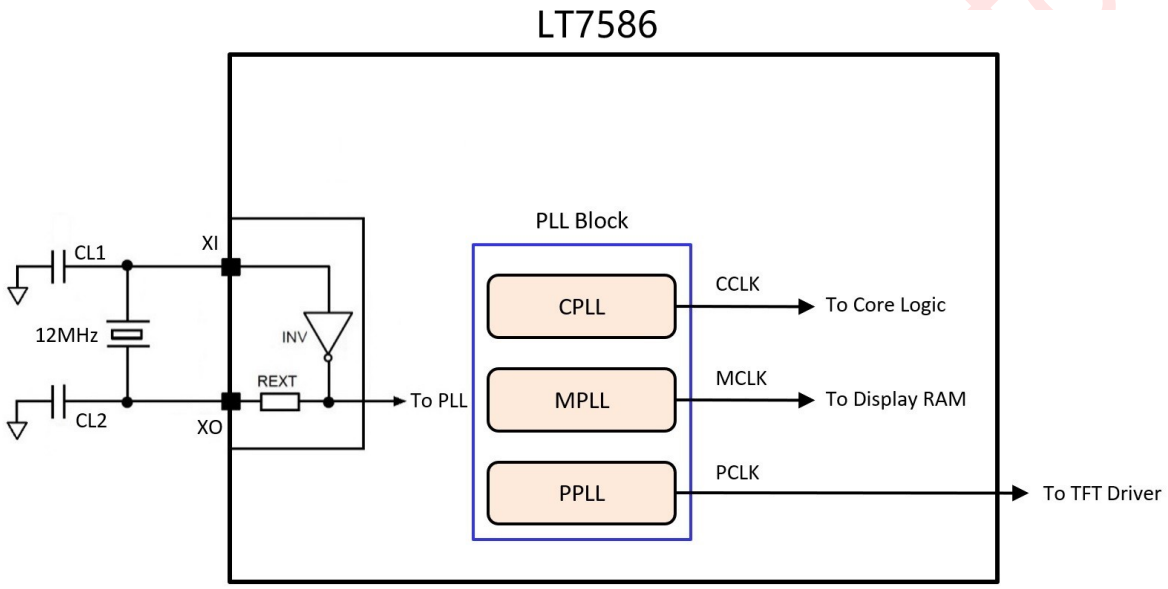


Figure 4-1: 3 Groups of PLL Circuits

The three PLL output frequencies are set by three independent PLL registers. F_{OUT} is the PLL output frequency of any group, and the formula is:

$$F_{OUT} = XI * (M \div N) \div OD$$

5. MCU Interface

LT7586 is controlled by an external MCU, and MCU directly reads and writes data to LT7586 registers or display RAM through the interface. LT7586 provides two 8-bit and 16-bit parallel interfaces, as well as SPI and I2C serial interfaces, allowing different MCUs to control LT7586 with suitable interfaces. The mode of the MCU interface is set by the PSM[2:0] pins. Please refer to the following table for settings:

Table 5-1: MCU Interface Mode Settings

PSM[2:0]	MCU Interface Mode
0 0 X	Select Parallel 8-bit Or 16-Bit 8080 Mode
0 1 X	Select Parallel 8-bit Or 16-Bit 6800 Mode
1 0 0	Select The Serial 3-Wire SPI Mode
1 0 1	Select The Serial 4-Wire SPI Mode (Supports By-Pass Mode)
1 1 0	Select Serial I2C Mode (Continuous Reading Mode Is Not Supported)
1 1 1	Select Serial I2C Mode (Support Continuous Reading Mode)

The following table is the MCU interface correspondence table supported by the LT7586 series:

Table 5-2: MCU Interfaces Supported by LT7586 Series

No.	MCU Interface Mode	LT7586B	LT7580
1	Parallel 8-bit 8080 Mode	V	V
2	Parallel 16-bit 8080 Mode	V	V
3	Parallel 8-bit 6800 Mode	V	--
4	Parallel 16-bit 6800 Mode	V	--
5	Serial 3-Wire SPI Mode	V	V
6	Serial 4-Wire SPI Mode	V	V
7	Serial I2C Mode	V	--

6. Display Memory

LT7586 has built-in display RAM. MCU stores the displayed data into the internal display RAM through instructions. LT7586 will continuously read the display data from the display RAM and send it to the TFT driver, so that the TFT Panel can present the image. The size of the display RAM capacity is related to the supported resolution and number of layers. The display RAM capacity supported by LT7586 is 128Mbits. The display RAM capacity, resolution and number of layers supported by each model are shown in the following table:

Table 6-1: LT7586 model and display memory capacity comparison table

Part Number	Embedded Display Memory	Resolution (Max.)	Color (Max.)	Number of Layers (@Max Color)
LT7586B	128Mbit	800*480	16.7M colors	1 4
		800*600	16.7M colors	11
		1024*600	16.7M colors	9
		1280*1024	16.7M colors	4
LT7580	128Mbit	800*480	16.7M colors	1 4
		800*600	16.7M colors	11
		1024*600	16.7M colors	9
		1024*768	16.7M colors	7

7. LCD Interface

LT7586 supports 16 and 24bits RGB interface panels. Whether it is 24bpp (RGB 8:8:8) or 16bpp (RGB 5:6:5) color, the signal can be sent to the driver on the TFT panel through these RGB interfaces.

Table 7-1: RGB Data Supported by LT7586's Model

Part Number	LCD Data Lines	RGB Data	Resolution	Color
LT7586B	PD[23~0]	R:G:B = 8:8:8	1280*1024	16.7M
	PD[23~19], PD[15~10], PD[7~3]	R:G:B = 5:6:5		65K
LT7580	PD[23~0]	R:G:B = 8:8:8	1024*768	16.7M
	PD[23~19], PD[15~10], PD[7~3]	R:G:B = 5:6:5		65K

The figure below is the interface timing diagram of LT7586 output to TFT-LCD. In addition to the above-mentioned PD data line, it also provides PCLK panel scan clock signal, VSYNC vertical synchronization signal, HSYNC horizontal synchronization signal, and PDE data enable signal.

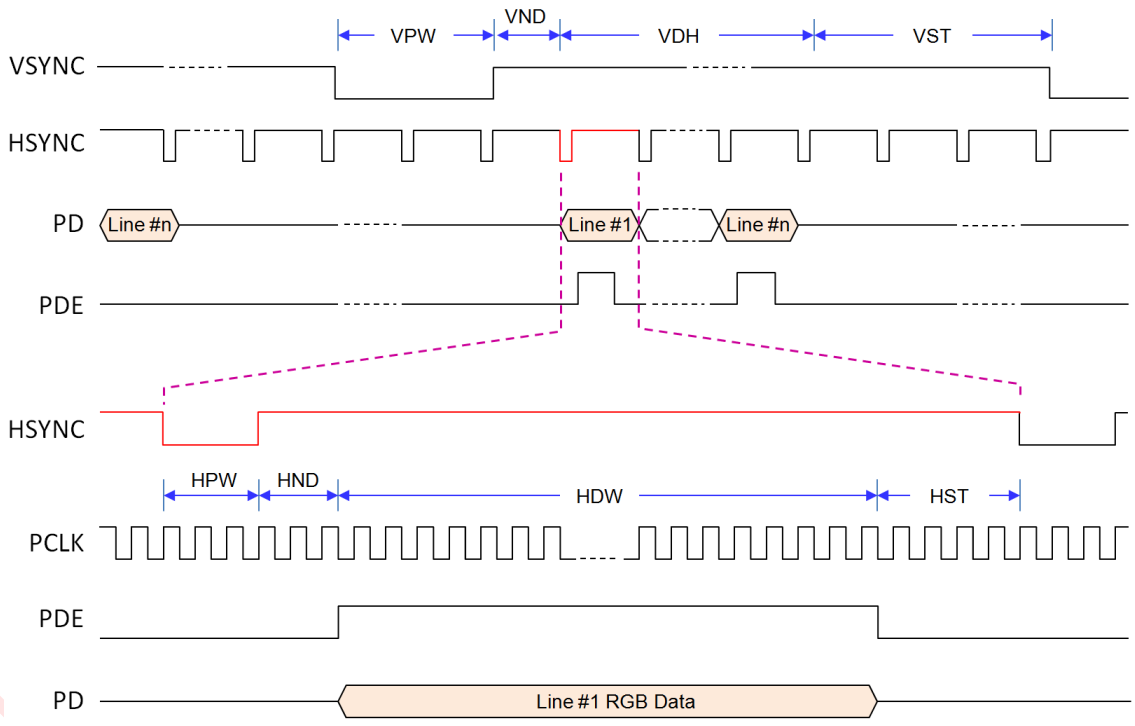


Figure 7-1: TFT-LCD RGB Interface Timing Diagram

8. Packaging Information

8.1 LT7586B (LQFP-128Pin)

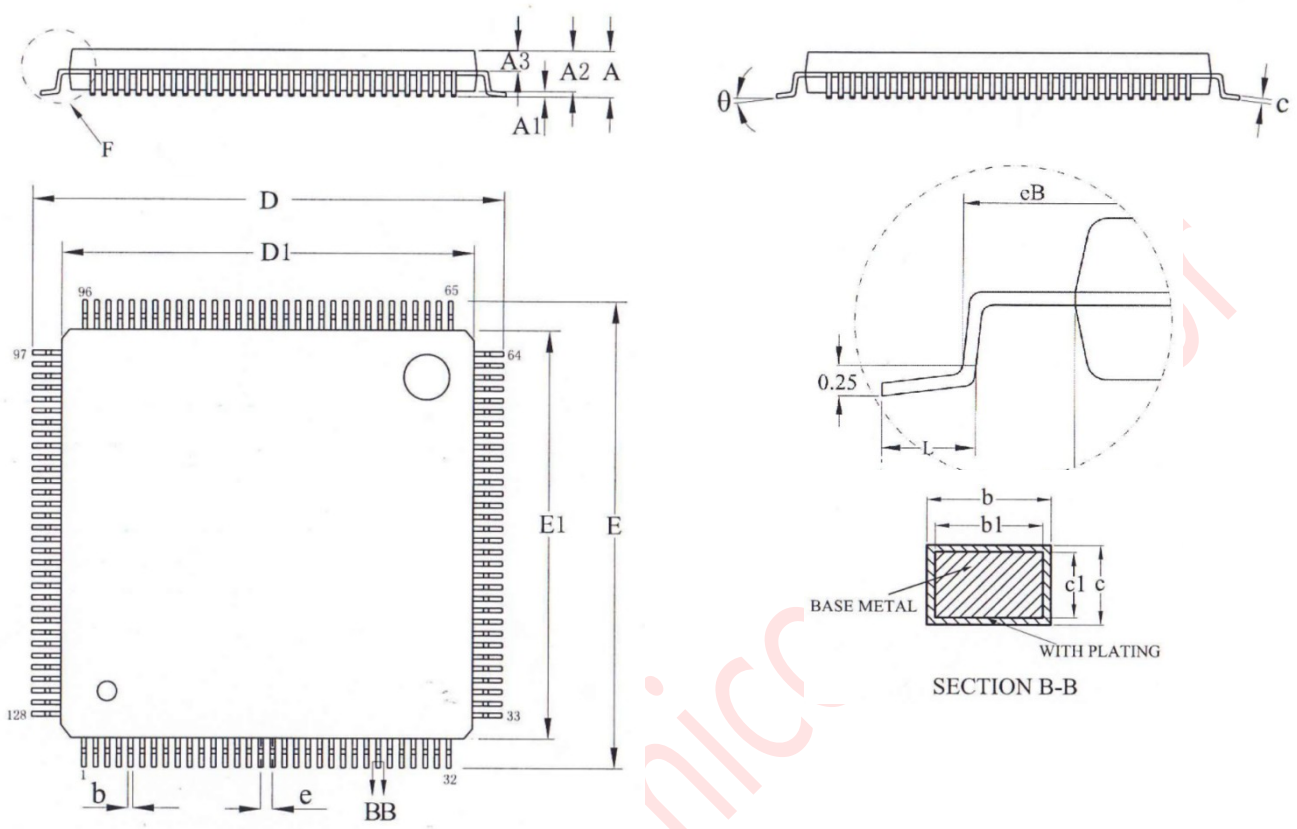


Figure 8-1: LQFP-128Pin Dimensions

Table 8-1: LQFP-128Pin Package Parameters

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	-	-	1.60	**D1**	13.9	14.0	14.1
A1	0.05	-	0.15	**E**	15.8	16.0	16.2
A2	1.35	1.40	1.45	**E1**	13.9	14.0	14.1
A3	0.59	0.64	0.69	**eB**	15.05	-	15.35
b	0.14	-	0.22	**e**	0.40 BSC		
b1	0.13	0.16	0.19	**L**	0.45	-	0.75
c	0.13	-	0.17	**L1**	1.00 REF		
c1	0.12	0.13	0.14	**θ**	0		7
D	15.8	16.00	16.2				

8.2 LT7580 (QFN-80pin)

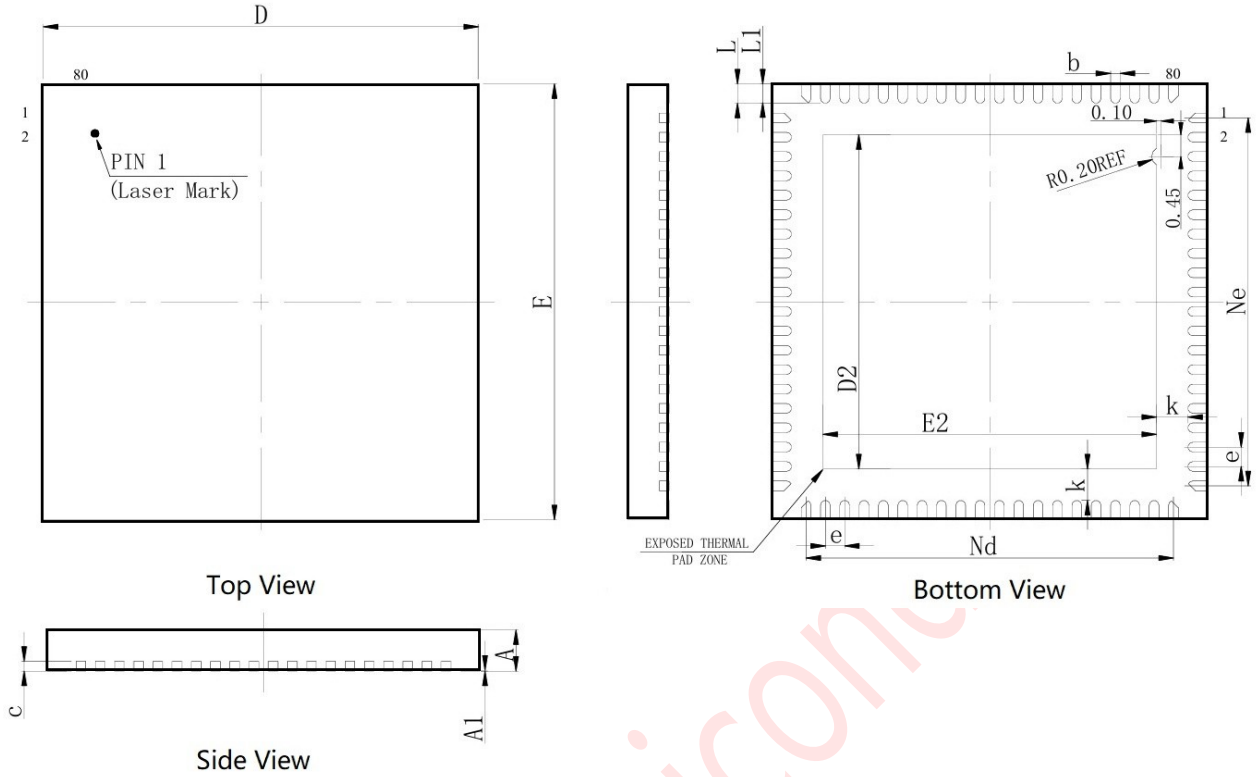


Figure 8-2: QFN-80Pin Dimensions

Note: When laying out the PCB, the thermal pad (Thermal Pad Zone) on the back of LT7580 must be directly grounded.

Table 8-2: QFN-80Pin Package Parameters

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	0.80	0.85	0.9	**Ne**	7.60BSC		
A1	0	0.02	0.05	**E**	8.90	9.00	9.10
b	0.15	0.20	0.25	**E2**	5.4	5.5	5.6
c	0.203REF			**L**	0.35	0.40	0.45
D	8.90	9.00	9.10	**L1**	0.29	0.39	0.49
D2	5.4	5.5	5.6	**K**	1.35REF		
e	0.40BSC			**h**	0.30	0.35	0.40
Nd	7.60BSC						

9. Reference Schematic

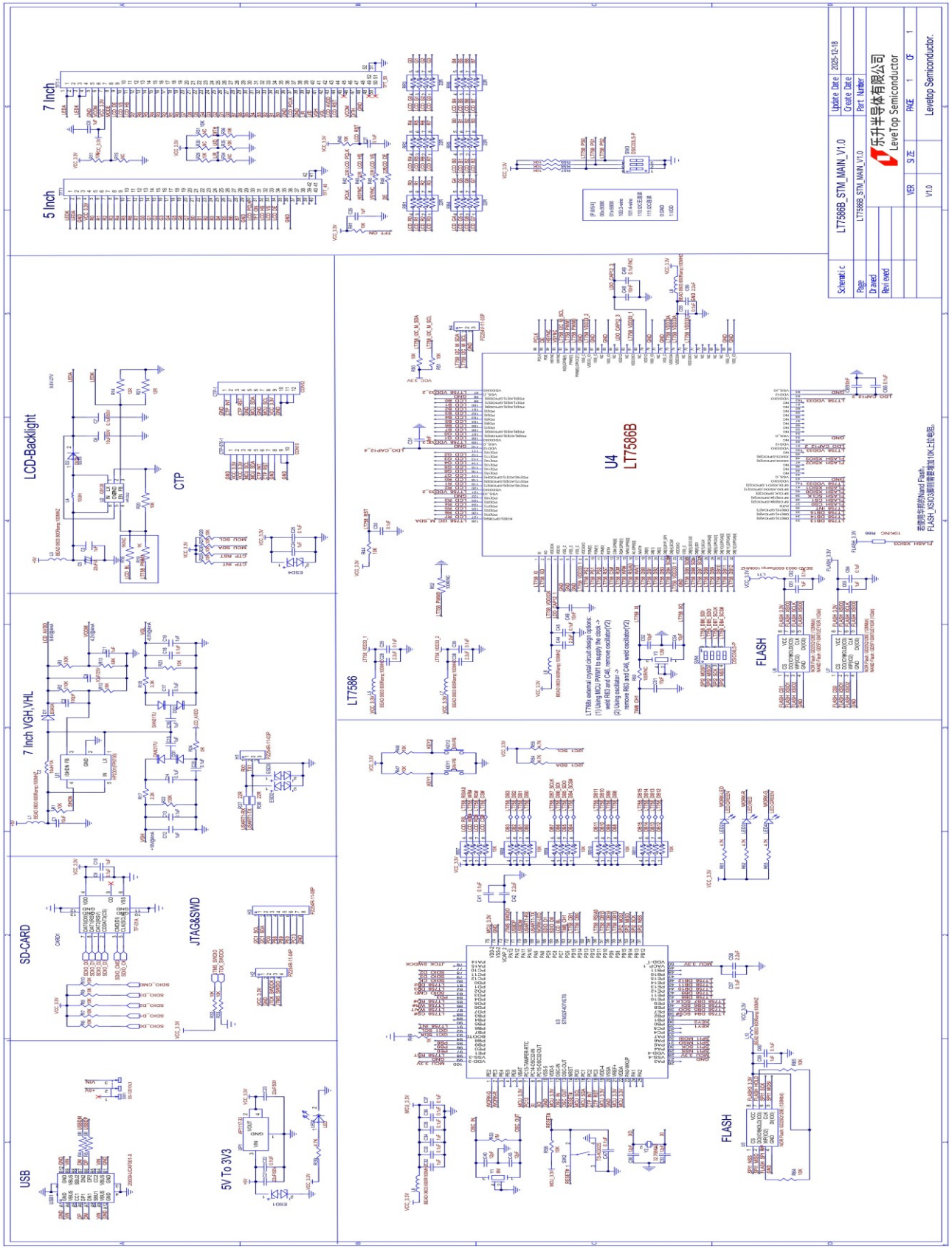


Figure 9-1: LT7586B Reference Schematic

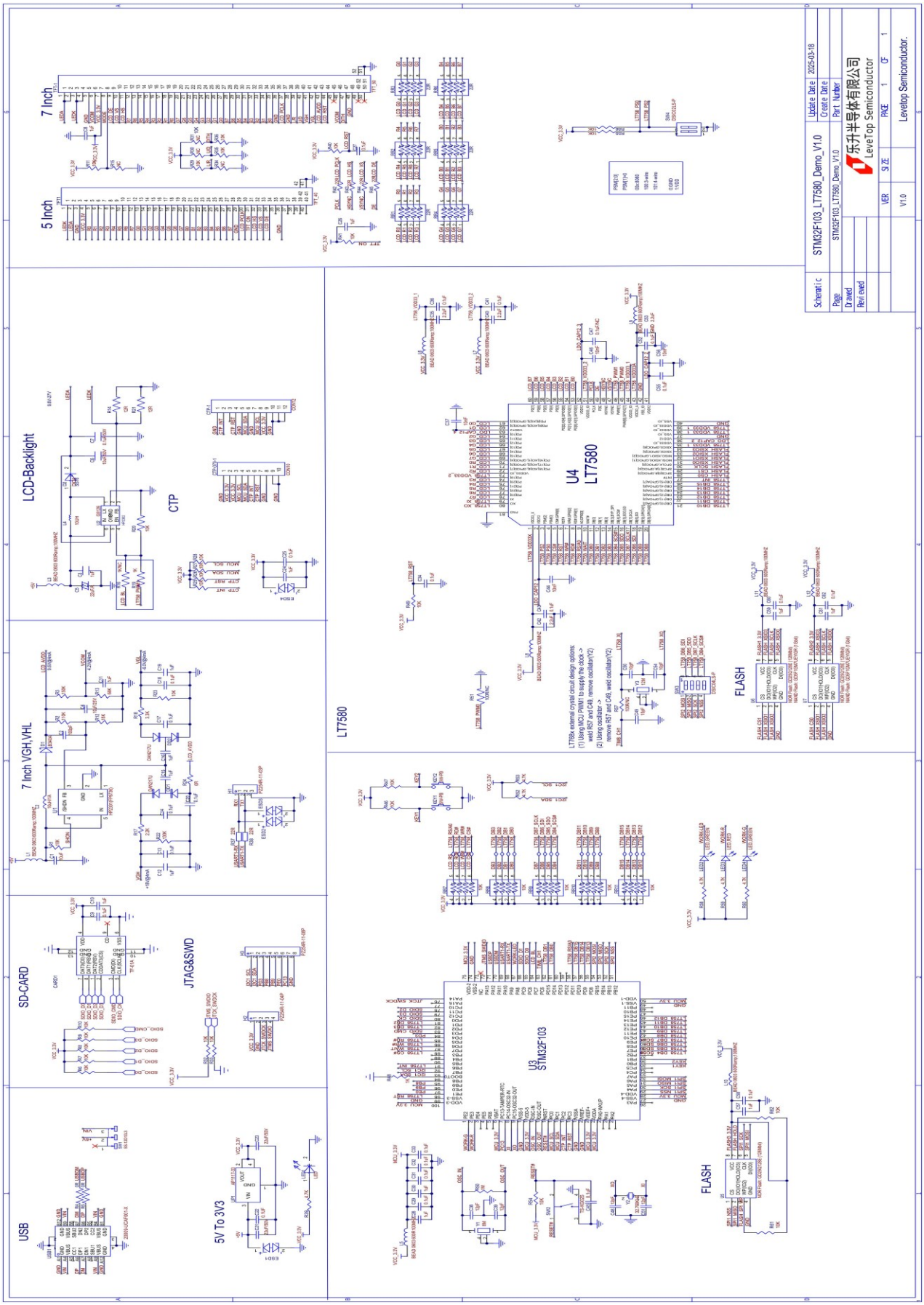


Figure 9-2: LT7580 Reference Schematic

