乐升半导体
LEVETOP

LT168

Uart TFT Display Controller

Brief Data Sheet

V2.1

www.levetop.cn
Levetop Semiconductor Co., Ltd.

Version History

Version	Date	Description
V1.0	2023/10/16	● Brief Data Sheet Release.
V1.1	2024/1/18	● Fixed the syntax errors described in the previous version. ● Update Section 2.3 Signal Properties Summary ● Update Chapter 6 Application Circuit
V1.2	2024/3/8	● Update Table 2-3 LT168x Comparison ● Update Chapter 6 Application Circuit
V1.5	2024/6/11	● Add Table 3-1 : The differences of LT168B for RGB Panel with or without PSRAM ● Add Section 5.4 VDD Power Up Timing ● Update Chapter 6 Application Circuit
V2.0	2024/8/16	● Update Table 3-1: The differences of LT168B for TFT Panel with or without PSRAM ● Add Section 7.3 PCB Design for Ground Pad
V2.1	2025/7/11	● Add Figure 3-16 Add Dedicated Reset Chip Reference Circuit

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1. LT168 Introduction

1.1. Introduction

LT168 is a serial Uart TFT display controller containing a built-in 32-bits MCU, Flash, and serial communication protocol. It supports TFT panels of max. 800*480 resolution, with SPI/QSPI or 8/16-bits parallel MCU interface and TFT panels of max. 480*480 resolution, with RGB interface.

LT168 supports the latest UI editing tool, UI_Editor-II, which enables developers to easily implement their display layout and operations through built-in widgets, such as displaying pictures, GIF, progress bar, trend chart, text, QRcode, and much more. Once the UI design is done, developers may export the bin file (UartTFT_Flash-II.bin) and program it to the external SPI flash connected to LT168. After power on, LT168 will then control the connected TFT panel to display the contents designed by the develpers. In addition, the host MCU may communicate with LT168 by sending predefined commands through Uart port. LT168 will then interpret the received commands and execute them. For more information, please refer to UI_Editor-II user manual.

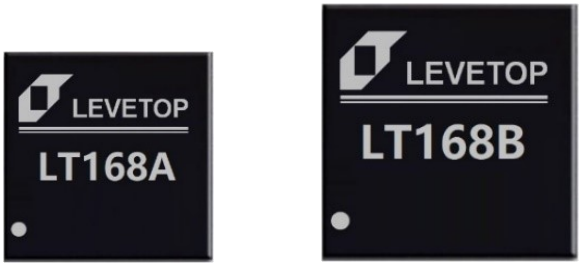
LT168 has an embedded 32-bits RISC core which can operate at maximum 200MHz frequency, high-speed memories (including 768K Bytes SRAM and 8K Bytes ROM), a 32K Bytes two-way set associative cache, Quad SPI Flash memory interface, an extensive range of enhanced peripherals and I/Os. All models offer standard communication interfaces (Master QSPI x 3, UARTs x 3, USB2.0 FS device x 1, I2C and CANBus controller x 1), EBI (External Bus Interface, support 8080 bus for 8080 MCU panels), a set of RGB Panel Interface, Timers (up to four general-purpose 16-bits timers, advanced-control PWM timer x 8, asynchronous Watch Dog Timer x 1, and RTC timers x 1), and analog modules (1MSPS ADC with 8-channels x 1 and Comparators x 2). LT168 also supports Little VGL for smooth display effects and good cost performance.

Benefiting from its high capacity Flash and SRAM, LT168 can be used as a master MCU as well. It is ideal for electronic products with small size TFT-LCD panel such as smart home appliances, handheld control equipment, industrial control panels, electronic instruments, medical equipment, small testing equipment, small electric motorcycles, personal medical beauty, small testing equipment, charging equipment, water and electricity meters, smart speakers with panel, etc.

The operating temperature range of LT168 is -40ºC to 105ºC, and the operating voltage is 3.3V. LT168 has two part numbers as listed below:

Table 1-1: LT168 Part Number

Part	Package	Embedded Flash	Embedded SRAM	TFT Panel Solution
LT168A	QFN48 (6*6 mm^2)	512K Bytes	256K Bytes + 512K Bytes	● 8-bits 8080 MCU Type TFT Display
LT168B	QFN68 (8*8 mm^2)	2M Bytes	256K Bytes + 512K Bytes	● 8/16-bits 8080 MCU Type TFT Display (Max. 800*480) ● QSPI Type TFT Display ● RGB 565 TFT Display (Max. 480*480)



QFN48 (6*6 mm^2) QFN68 (8*8 mm^2)

Figure 1-1: LT168A and LT168B Outline

1.2. Internal Block Diagram

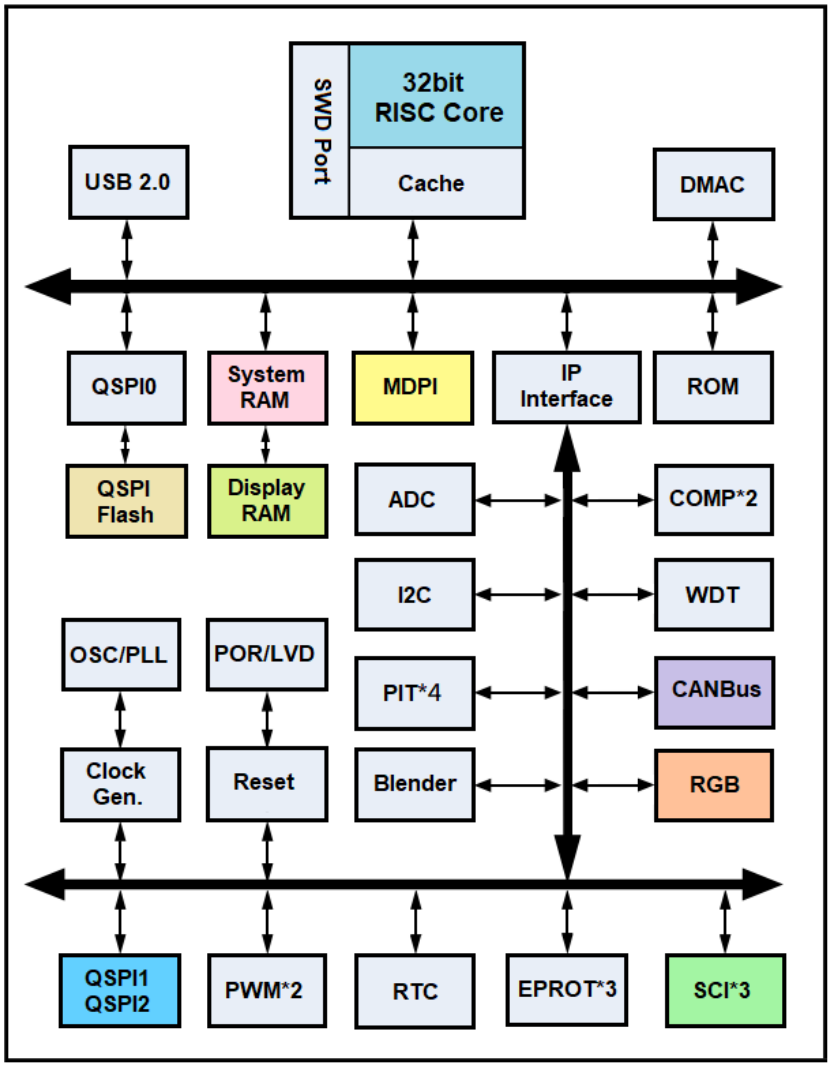


Figure 1-2: **Internal Block Diagram**

1.3. Features

1.3.1. 32-bits RISC Processor

– 32-bits load/store reduced instruction set computer (RISC) architecture with fixed 16-bits instruction length
– 16 entry 32-bits general-purpose register file
– Efficient 3-stage execution pipeline, hidden from application software
– Single-cycle instruction execution for many Instructions, three cycles for branches
– Support for byte/halfword/word memory accesses
– Embedded interrupt controller, support nested vector interrupts
– Single-cycle 32-bits x 32-bits hardware integer multiplier array
– 3~13 cycles hardware integer divider array

1.3.2. On-chip 768K Bytes Of Static Random-Access Memory (SRAM)

– Single cycle byte, half-word (16-bits), and word (32-bits) reads and writes
– Two segment for improving performance at certain application
  • System RAM: 256K Bytes and address range from 0x800000 to 0x83FFFF.
  • Display RAM: 512K Bytes and address range from 0x840000 to 0x8BFFFF

1.3.3. On-chip QSPI Flash

– LT168A embedded 512K Bytes QSPI Flash, support Levetop's Communication Program
– LT168B embedded 2M Bytes QSPI Flash, support Levetop's Communication Program

1.3.4. 8K Bytes Of Static Read-Only Memory (ROM)

– Single cycle byte, half-word (16-bits), and word (32-bits) reads access

1.3.5. 32K Bytes Of Cache Memory

– 2-way set -associative organization
– Two AHB bus interfaces, a master and a slave interface

1.3.6. External Bus Interface (EBI)

– Programmable wait states -up to 16 wait states can be programmed before the access terminated
– One programmable asynchronous active-low chip selects.
– Programmable chip selects wait cycle
  • To interface with various panels, up to 16 chip selects asserted cycle can be programmed
– Programmable read/write asserted cycle
– Programmable read/write negated cycle
– Support 8/16-bits port size.
– Support 8080 standard bus
– Support 8080 Parallel Type TFT Panel:
  • 800 x 480
  • 480 x 272
  • 480 x 320
  • 320 x 240 or Less

1.3.7. RGB Display Panel Interface

– Data frame format: Red: 5, Green: 6, Blue: 5
– Supported resolution ratio:
  • 480 x 480
  • 480 x 272 or Less
– Timing of the interface signals is configurable
  • Polarity and pixel clock polarity is configurable

1.3.8. DMA Controller

– 32 independent programmable DMA controller channels
– Data transfers in 8, 16, 32-bits
– Support single transfer, Burst 4, 8,16 transfer, and burst always under a special case.
– Support single cycle transfer
– Support automatic transfer mode
– Support LLI transfer mode
– Follow a fixed priority rule

1.3.9. Reset Function

– Internal power on reset circuit
– Five sources of reset:
  • Power-on Reset
  • External Pin
  • Software Reset
  • Watchdog Timer
  • Program Voltage Detect Reset
– Status flag indicates source of the last reset

1.3.10. Four Periodic Interval Timer

– 16-bits counter with modulus "initial count" register
– Selectable as free running or count down
– 16 selectable prescalers — 2^0 to 2^{15}
– Support DMA interface

1.3.11. One Watchdog Timer

– 16-bits counter with modulus "initial count" register
– Pause option for low-power modes
– Up to 2000ms service time

1.3.12. One RTC Timer

– Support loading time data to and reading time data from seconds, minutes, hours and days counters
– Support alarm settings
– Interrupt sources:
  • Second, Minute, Hour, Day interrupts
  • Programmable alarm interrupts
  • 1KHz/32KHz periodic interrupts

1.3.13. Three External Interrupts Port (EPORT)

– Eight Channels for each EPORT
– Rising/falling edge select
– Low/High level sensitive
– Interrupt pins configurable as general-purpose I/O

1.3.14. Three Quad Serial Peripheral Interface Master Module (QSPI)

– Serial-master operation
– DMA controller interface
– Enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
– Clock stretching support in enhanced SPI transfers
– Data item size (4 to 32-bits) – Item size of each data transfer is under control of the programmer
– Configurable depth of the transmit and receive FIFO buffers from 2 to 256 words deep. The FIFO width is fixed at 32-bits
– Enhanced SPI support
– Execute in Place (XIP) mode support

1.3.15. Three Serial Communications Interface Module (SCI)

– Full-duplex, standard non-return-to-zero (NRZ) format
– Programmable baud rates (13-bits modulo divider) with configurable oversampling ratio from 4x to 256x
– Interrupt, polled operation
  • Transmit data register empty and transmission complete
  • Receive data register full
  • Receive overrun, parity error, framing error, and noise error
  • Idle receiver detect
  • Active edge on receive pin
  • Break detect supporting LIN
  • Receive Data Match
– Hardware parity generation and checking
– Programmable 8-bits, 9-bits or 10-bits character length
– Programmable 1-bit or 2-bits stop bits
– Three receiver wakeup methods:
  • Idle line wakeup
  • Address mark wakeup
  • Receive data match

– Automatic address matching to reduce ISR overhead:
  • Address mark matching
  • Idle line address matching
  • Address Match Start, Address Match End
– Optional 13-bits break character generation / 11-bits break character detection
– Configurable idle length detection, supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
– Selectable transmitter output and receiver input polarity
– Selectable IrDA 1.4 Return-to-Zero-Inverted (RZI) format with programmable pulse width
– Independent FIFO structure for “transmit” and “receive”
  • Separate configurable watermark for “receive“ and “transmit“ requests
  • Option for receiver to assert request after a configurable number of idle characters if the “receive“ FIFO is not empty

1.3.16. One Canbus Controller:

– Full implementation of the CAN protocol specification, version 2.0B
  • Standard data and remote frames
  • Extended data and remote frames
  • 0–8 bytes data length
  • Programmable bit rate up to 1 Mbit/s
  • Content-related addressing
– 64 Message Buffers of zero to eight bytes data length
– Each MB configurable as Rx or Tx, all supporting standard and extended messages
– Individual Rx Mask Registers per Message Buffer
– Includes either 1056 bytes (64 MBs) of SRAM used for MB storage
– Includes either 256 bytes (64 MBs) of SRAM used for individual Rx Mask Registers
– Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
– Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8-bits) IDs, with individual masking capability
– Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
– Unused MB and Rx Mask Register space can be used as general purpose SRAM space
– Listen-only mode capability
– Programmable loop-back mode supporting self-test operation
– Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
– Time Stamp based on 16-bits free-running timer
– Global network time, synchronized by a specific message
– Maskable interrupts
– Independent of the transmission medium (an external transceiver is assumed)
– Short latency time due to an arbitration scheme for high-priority messages
– Low power mode
– Hardware cancellation on Tx message buffers

1.3.17. One Usb2.0 Full Speed Compatible Device (USB)

– Supports internal reference clock or external 12MHz crystal reference clock
– Compliant with USB2.0 full speed specification with on-chip integrated PHY module
– Supports FS (12Mbps) mode
– Supports up to 8 endpoints, including endpoint 0
– All endpoints except endpoint 0 can support interrupt and bulk transfer
– All endpoints except endpoint 0 can be configured as 8, 16, 32, 64 bytes FIFO size
– Endpoint 0 supports control transfer

1.3.18. Two Pulse Width Modulator (PWM)

– Four channel each PWM controller
– Programmable period
– Programmable duty cycle
– Two Dead-Zone generator
– Capture function
– Pins can be configured as general-purpose I/O

1.3.19. ADC With 8-Channel

– High performance
  • 12-bits, 10-bits, 8-bits or 6-bits configurable resolution
  • ADC conversion time: 1.0 μs for 12-bits resolution (1 MHz), 0.88 μs conversion time for 10-bits resolution, faster conversion times can be obtained by lowering resolution.
  • Programmable sampling time
  • Data alignment with built-in data coherency
  • DMA support

– Low power
  • PLCK frequency can be reduced for low power operation while still keeping optimum ADC performance. For example, 1.0 μs conversion time is kept, whatever the frequency of PLCK
  • Wait mode: to prevent ADC overrun in applications under low frequency PLCK
  • Auto off mode: ADC is automatically powered off except during the active conversion phase. This dramatically reduces the power consumption of the ADC.

– Analog input channels
  • 8 external analog inputs

– Start-of-conversion can be initiated:
  • By software
  • By hardware triggers with configurable polarity

– Conversion modes
  • Can convert a single channel or can scan a sequence of channels.
  • Single mode converts selected inputs once per trigger
  • Continuous mode converts selected inputs continuously
  • Discontinuous mode

– Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events.
– Analog watchdog
– Single-ended and differential-input configurations Converter uses an internal reference or an external reference

1.3.20. Two Analog Comparators

– Programmable response time
– Programmable hysteresis
– Support analog input multiplexer with nine selection
– Two optional output: filtered or asynchronous output
– Selectable rising/falling edge interrupt

1.3.21. Power Management Unit (PMU)

– Support on-chip 1.2V LDO with maximum load current 100mA
– 1.2V LDO support two mode: lower power, high power

1.3.22. Programmable Voltage Detector

– Programmable voltage detector

1.3.23. Internal Oscillator

– 128KHz on-chip oscillator clock for watchdog and PMU
– PLL clock which can be used for system clock
– 48MHz USB PLL clock which can be used for USB SIE

1.3.24. External Crystal Oscillator

– Up to 20Mhz external crystal Oscillator clock which can be used for system clock
– 32.768Khz external crystal Oscillator clock which can be used for RTC

1.4. System Block

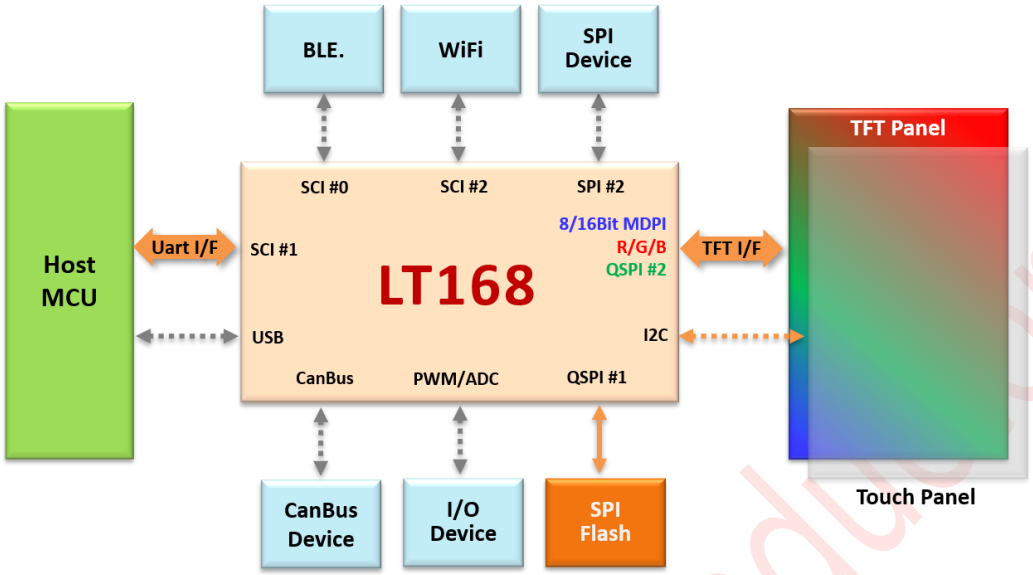


Figure 1-3: System Block of LT168

1.5. Application Diagram

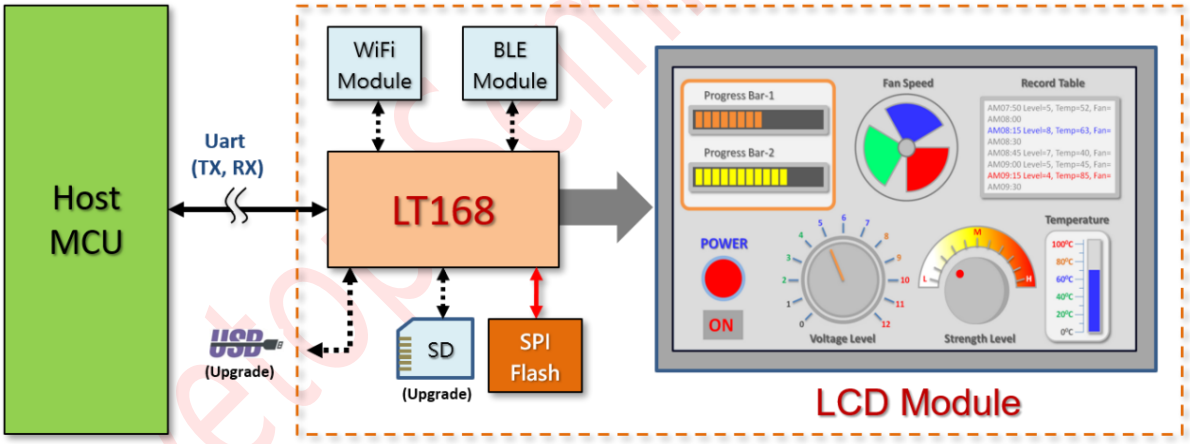


Figure 1-4: Application Diagram of TFT LCD Module

2. Signal Description

2.1. Introduction

LT168 is available in the following packages:

- QFN48 (6*6 mm^2) – LT168A
- QFN68 (8*8 mm^2) – LT168B

2.2. Pin Assignment

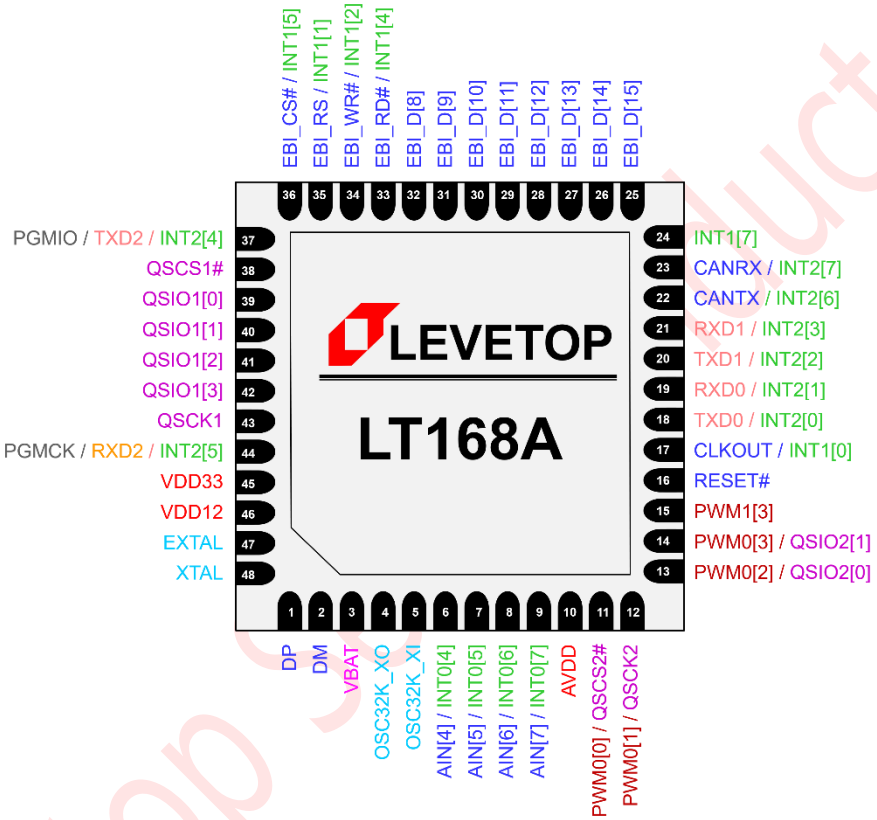


Figure 2-1: LT168A (QFN48) Pin Assignment

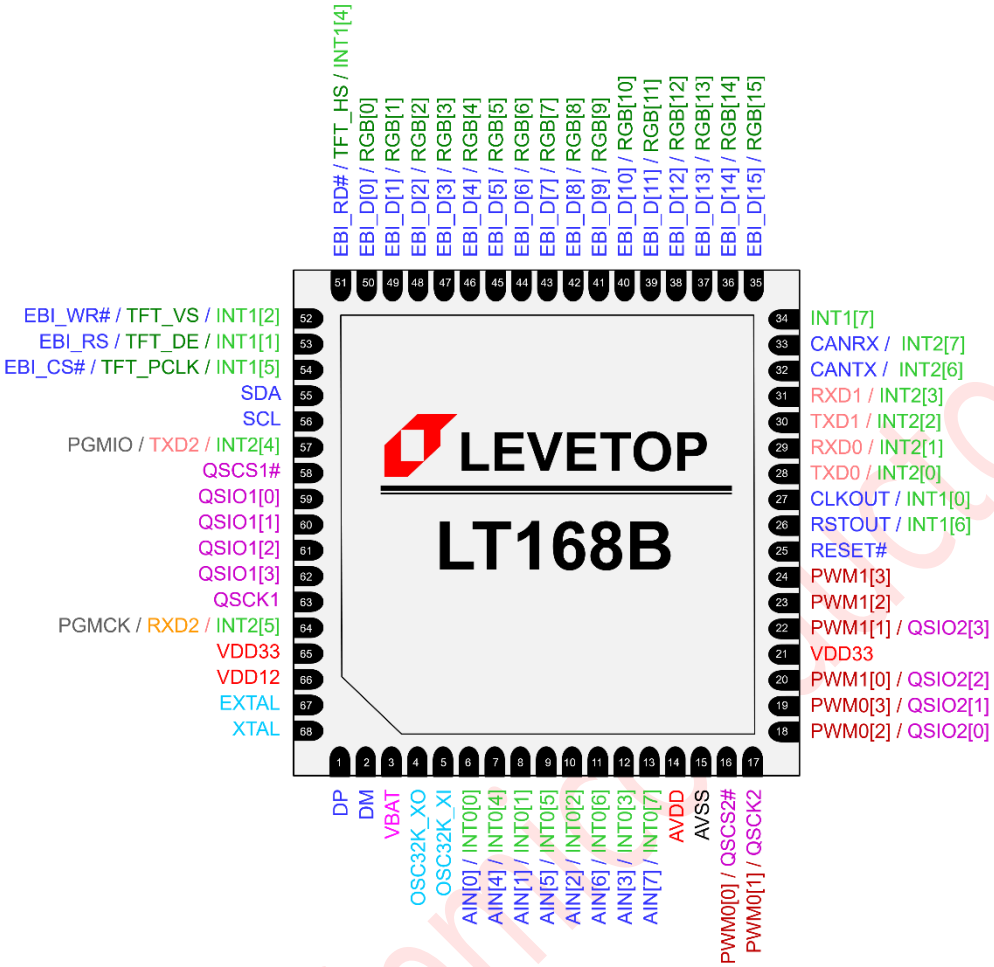


Figure 2-2: LT168B (QFN68) Pin Assignment

2.3. Signal Properties Summary

Table 2-1: Signal Properties

Name	Alternate 0	Alternate 1	Pin #		Qty.	Dir.	Default Dir *2	Pullup *3	IO Type *4
			LT168A	LT168B					
SCI (6)									
RXD0 *1	INT2[1]	-	19	29	1	I/O	I	PullUp	PBCUL16R
TXD0	INT2[0]	-	18	28	1	I/O	O(H)	-	PBCUL16R
RXD1	INT2[3]	-	21	31	1	I/O	I	PullUp	PBCUL16R
TXD1	INT2[2]	-	20	30	1	I/O	O(H)	-	PBCUL16R
RXD2	PGMCK	INT2[5]	44	64	1	I/O	I	PullUp	PBCUL16R
TXD2	PGMIO	INT2[4]	37	57	1	I/O	I	PullUp	PBCUL16R
USB (2)									
DP	-	-	1	1	1	Analog	Hiz	-	-
DM	-	-	2	2	1	Analog	Hiz	-	-
I2C (2)									
SCL	GPIO_SCL	-	-	56	1	I/O	I	PullUp	PBCUL16R
SDA	GPIO_SDA	-	-	55	1	I/O	I	PullUp	PBCUL16R
QSPI (18)									
QSIO2[3]	PWM1[1]	-	-	22	1	I/O	I	PullDown	PBCD24R
QSIO2[2]	PWM1[0]	-	-	20	1	I/O	I	PullDown	PBCD24R
QSIO2[1]	PWM0[3]	-	14	19	1	I/O	I	PullDown	PBCD24R
QSIO2[0]	PWM0[2]	-	13	18	1	I/O	I	PullDown	PBCD24R
QSCK2	PWM0[1]	-	12	17	1	I/O	I	PullDown	PBCD24R
QSCS2#	PWM0[0]	-	11	16	1	I/O	I	PullDown	PBCD24R
QSIO1[3]	-	-	42	62	1	I/O	I	PullUp	PBCU24R
QSIO1[2]	-	-	41	61	1	I/O	I	PullUp	PBCU24R
QSIO1[1]	-	-	40	60	1	I/O	I	PullUp	PBCU24R
QSIO1[0]	-	-	39	59	1	I/O	I	PullUp	PBCU24R
QSCK1	-	-	43	63	1	O	O(L)	-	PBCU24R
QSCS1#	-	-	38	58	1	O	O(H)	-	PBCU24R
QSIO0[3] *5	-	-	-	-	1	I/O	I	PullUp	PBCU24R
QSIO0[2]	-	-	-	-	1	I/O	I	PullUp	PBCU24R
QSIO0[1]	-	-	-	-	1	I/O	I	PullUp	PBCU24R
QSIO0[0]	-	-	-	-	1	I/O	I	PullUp	PBCU24R
QSCK0	-	-	-	-	1	O	O(L)	-	PBCU24R
QSCS0#	-	-	-	-	1	O	O(H)	-	PBCU24R
PWM0 (4)									
PWM0[3]	QSIO2[1]	-	14	19	1	I/O	I	PullDown	PBCD24R
PWM0[2]	QSIO2[0]	-	13	18	1	I/O	I	PullDown	PBCD24R

Name	Alternate 0	Alternate 1	Pin #		Qty.	Dir.	Default Dir *2	Pullup *3	IO Type *4
			LT168A	LT168B					
PWM0[1]	QSCK2	-	12	17	1	I/O	I	PullDown	PBCD24R
PWM0[0]	QSCS2#	-	11	16	1	I/O	I	PullDown	PBCD24R
PWM1 (4)									
PWM1[3]	-	-	15	24	1	I/O	I	PullDown	PBCD24R
PWM1[2]	-	-	-	23	1	I/O	I	PullDown	PBCD24R
PWM1[1]	QSIO2[3]	-	-	22	1	I/O	I	PullDown	PBCD24R
PWM1[0]	QSIO2[2]	-	-	20	1	I/O	I	PullDown	PBCD24R
ADC (8)									
AIN[7]	INT0[7]	-	9	13	1	Analog	Hiz	-	PVDD1ANPR
AIN[6]	INT0[6]	-	8	11	1	Analog	Hiz	-	PVDD1ANPR
AIN[5]	INT0[5]	-	7	9	1	Analog	Hiz	-	PVDD1ANPR
AIN[4]	INT0[4]	-	6	7	1	Analog	Hiz	-	PVDD1ANPR
AIN[3]	INT0[3]	-	-	12	1	Analog	Hiz	-	PVDD1ANPR
AIN[2]	INT0[2]	-	-	10	1	Analog	Hiz	-	PVDD1ANPR
AIN[1]	INT0[1]	-	-	8	1	Analog	Hiz	-	PVDD1ANPR
AIN[0]	INT0[0]	-	-	6	1	Analog	Hiz	-	PVDD1ANPR
Edge Port 0 (8)									
INT0[7]	AIN[7]	-	9	13	1	I/O	Hiz	-	PBCUL16R
INT0[6]	AIN[6]	-	8	11	1	I/O	Hiz	-	PBCUL16R
INT0[5]	AIN[5]	-	7	9	1	I/O	Hiz	-	PBCUL16R
INT0[4]	AIN[4]	-	6	7	1	I/O	Hiz	-	PBCUL16R
INT0[3]	AIN[3]	-	-	12	1	I/O	Hiz	-	PBCUL16R
INT0[2]	AIN[2]	-	-	10	1	I/O	Hiz	-	PBCUL16R
INT0[1]	AIN[1]	-	-	8	1	I/O	Hiz	-	PBCUL16R
INT0[0]	AIN[0]	-	-	6	1	I/O	Hiz	-	PBCUL16R
Edge Port 1 (7)									
INT1[7]	-	-	24	34	1	I/O	I	PullUp	PBCUL16R
INT1[6]	RSTOUT	-	-	26	1	I/O	O	-	PBCUL16R
INT1[5]	EBI_CS#	TFT_PCLK	36	54	1	I/O	O(H)	-	PBCU24R
INT1[4]	EBI_RD#	TFT_HS	33	51	1	I/O	O(H)	-	PBCU24R
INT1[2]	EBI_WR#	TFT_VS	34	52	1	I/O	O(H)	-	PBCU24R
INT1[1]	EBI_RS	TFT_DE	35	53	1	I/O	O(L)	-	PBCU24R
INT1[0]	CLKOUT	-	17	27	1	I/O	O	-	PBCUL16R
Edge Port 2 (8)									
INT2[7]	CANRX	-	23	33	1	I/O	I	PullUp	PBCUL16R
INT2[6]	CANTX	-	22	32	1	I/O	O(H)	-	PBCUL16R

Name	Alternate 0	Alternate 1	Pin #		Qty.	Dir.	Default Dir *2	Pullup *3	IO Type *4
			LT168A	LT168B					
INT2[5]	RXD2	PGMCK	44	64	1	I/O	I	PullUp	PBCUL16R
INT2[4]	TXD2	PGMIO	37	57	1	I/O	I	PullUp	PBCUL16R
INT2[3]	RXD1	-	21	31	1	I/O	I	PullUp	PBCUL16R
INT2[2]	TXD1	-	20	30	1	I/O	O(H)	-	PBCUL16R
INT2[1]	RXD0	-	19	29	1	I/O	I	PullUp	PBCUL16R
INT2[0]	TXD0	-	18	28	1	I/O	O(H)	-	PBCUL16R
Programming Port (2)									
PGMCK	RXD2	INT2[5]	44	64	1	I/O	I	PullUp	PBCUL16R
PGMIO	TXD2	INT2[4]	37	57	1	I/O	I	PullUp	PBCUL16R
CLOCK (5)									
EXTAL	-	-	47	67	1	I/O	I	-	PXWE2R
XTAL	-	-	48	68	1	I/O	O	-	PXWE2R
OSC32K_XI	-	-	5	5	1	I/O	I	-	PVDD1ANPR
OSC32K_XO	-	-	4	4	1	I/O	O	-	PVDD1ANPR
CLKOUT	INT1[0]	-	17	27	1	I/O	O	-	PBCUL16R
RESET (2)									
RESET#	-	-	16	25	1	-	I	PullUp	PISUR
RSTOUT	INT1[6]	-	-	26	1	I/O	O	-	PBCUL16R
CAN (2)									
CANRX	INT2[7]	-	23	33	1	I/O	I	PullUp	PBCUL16R
CANTX	INT2[6]	-	22	32	1	I/O	O(H)	-	PBCUL16R
EBI (20)									
EBI_CS# *6	TFT_PCLK	INT1[5]	36	54	1	I/O	O(H)	-	PBCU24R
EBI_RS	TFT_DE	INT1[1]	35	53	1	I/O	O(L)	-	PBCU24R
EBI_RD#	TFT_HS	INT1[4]	33	51	1	I/O	O(H)	-	PBCU24R
EBI_WR#	TFT_VS	INT1[2]	34	52	1	I/O	O(H)	-	PBCU24R
EBI_D[15]	TFT_RGB[15]	GPIO_D[15]	25	35	1	I/O	I	PullUp	PBCU24R
EBI_D[14]	TFT_RGB[14]	GPIO_D[14]	26	36	1	I/O	I	PullUp	PBCU24R
EBI_D[13]	TFT_RGB[13]	GPIO_D[13]	27	37	1	I/O	I	PullUp	PBCU24R
EBI_D[12]	TFT_RGB[12]	GPIO_D[12]	28	38	1	I/O	I	PullUp	PBCU24R
EBI_D[11]	TFT_RGB[11]	GPIO_D[11]	29	39	1	I/O	I	PullUp	PBCU24R
EBI_D[10]	TFT_RGB[10]	GPIO_D[10]	30	40	1	I/O	I	PullUp	PBCU24R
EBI_D[9]	TFT_RGB[9]	GPIO_D[9]	31	41	1	I/O	I	PullUp	PBCU24R
EBI_D[8]	TFT_RGB[8]	GPIO_D[8]	32	42	1	I/O	I	PullUp	PBCU24R
EBI_D[7]	TFT_RGB[7]	GPIO_D[7]	-	43	1	I/O	I	PullUp	PBCU24R
EBI_D[6]	TFT_RGB[6]	GPIO_D[6]	-	44	1	I/O	I	PullUp	PBCU24R

Name	Alternate 0	Alternate 1	Pin #		Qty.	Dir.	Default Dir *2	Pullup *3	IO Type *4
			LT168A	LT168B					
EBI_D[5]	TFT_RGB[5]	GPIO_D[5]	-	45	1	I/O	I	PullUp	PBCU24R
EBI_D[4]	TFT_RGB[4]	GPIO_D[4]	-	46	1	I/O	I	PullUp	PBCU24R
EBI_D[3]	TFT_RGB[3]	GPIO_D[3]	-	47	1	I/O	I	PullUp	PBCU24R
EBI_D[2]	TFT_RGB[2]	GPIO_D[2]	-	48	1	I/O	I	PullUp	PBCU24R
EBI_D[1]	TFT_RGB[1]	GPIO_D[1]	-	49	1	I/O	I	PullUp	PBCU24R
EBI_D[0]	TFT_RGB[0]	GPIO_D[0]	-	50	1	I/O	I	PullUp	PBCU24R
Power Supply									
VDD33	-	-	45	21, 65	2	P	-	-	PVDD2R
VDD12	-	-	46	66	1	P	-	-	PWR
AVDD	-	-	10	14	1	P	-	-	PVDD1ANPR
VBAT	-	-	3	3	1	P	-	-	PWR
VSS	-	-	49*7	69*7	1	G	-	-	PWR
AVSS	-	-	-	15	1	G	-	-	PWR

Notes:

1. The Red signal name is the default signal for the multi-purpose pin.

2. "Default Dir" is referred to direction after Reset. "I" stands for Input, "O" stands for Output, "O(H)" stands for Output High, "O(L)" stands for Output Low, and "Hiz" means Input and Output are all disabled and pullup/pulldown is also dis-abled.

3. All pullups and pulldowns are disconnected when the signal is programmed as an output.

4. Output Driver Type:

   - PBCU24R = CMOS Tri-state output pad with controllable input and controllable pull-up,
   - PBCUL16R = CMOS Tri-state output pad with controllable input and controllable pullup and limited slew rate,
   - PBCD24R = CMOS Tri-state output pad with enable controlled input and enable controlled pull down,
   - PISUR = schmitt trigger enable controlled input pad with pull-up,
   - PVDD1ANPR = VDD analog PAD with digital power domain,
   - PXWE2R = Crystal oscillator with internal resistor and active high enable,
   - PVDD2R = VDD power pad for I/O post driver,
   - The suffix of cell means the drive strength and x can be 2, 16 and 24. For example, PBCU24R means the drive strength is 24mA.

5. These QSPI0 signals are connected directly to the embedded SPI Flash memory.

6. The control signals of the "EBI Bus" are dedicated hardware interface and cannot be replaced by other GPIO pins.

7. This is the back thermal pad of the LT168x. It must connect to ground (VSS/GND) directly.

2.4. Signal Descriptions

This subsection provides a brief description of the signals. For more detailed information, reference the specific module section.

Table 2-2: Signal Description

Pin Name	Pin Number		Pin Description
	LT168A	LT168B	
Serial Communications Interface 0 Module Signals (SCI0)			
RXD0	19	29	**Receive Data** This signal can be configured as the SCI0 receiver data input, or be configured as GPIO (INT2[1]).
TXD0	18	28	**Transmit Data** This signal can be configured as the SCI0 transmitter data output, or be configured as GPIO (INT2[0]).
Serial Communications Interface 1 Module Signals (SCI1)			
RXD1	21	31	**Receive Data** This signal can be configured as SCI1 receiver data input, or be configured as GPIO (INT2[3]) .
TXD1	20	30	**Transmit Data** This signal can be configured as SCI1 transmitter data output, or be configured as GPIO (INT2[2]) .
Serial Communications Interface 2 Module Signals (SCI2)			
RXD2	44	64	**Receive Data** This signal can be configured as SCI2 receiver data input, GPIO (INT2[5]) or PGMCK
TXD2	37	57	**Transmit Data** This signal can be configured as SCI2 transmitter data output, GPIO (INT2[4]) or PGMIO.
CAN Module Signals			
CANRX	23	33	**Receive Data** This pin is the receive pin from the CANBus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'. This signal can also be used as GPIO (INT2[7]) when not configured for Canbus operation.
CANTX	22	32	**Transmit Data** This pin is the transmit pin to CANBus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'. This signal can also be used as GPIO (INT2[6]) when not configured for Canbus operation.

Pin Name	Pin Number		Pin Description
	LT168A	LT168B	
RGB Controller Module Signals These signals are available for LT168B only, and are used to drive RGB type TFT panel.			
TFT_PCLK	-	54	**TFT Pixel Clock** This is pixel clock used to drive the display panel.
TFT_HS	-	51	**TFT Horizontal Synchronous Signal** This is horizontal synchronous signal, indicating the beginning of a new line.
TFT_VS	-	52	**TFT Vertical Synchronous Signal** This is vertical synchronous signal, indicating the beginning of a new frame.
TFT_DE	-	53	**TFT Data Enable** This is data enable signal for RGB interface operation.
TFT_RGB[15:0]	-	35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50	**TFT RGB Signals** This is Red, Green and Blue data output.
External Bus Interface (EBI) Signals The External Bus Interface (EBI) is responsible for controlling the transfer of the information between the internal bus and the external 8080 Parallel MCU Panel. LT168A supports 8-bits EBI, and LT168B supports 8-bits or 16-bits EBI.			
EBI_CS#	36	54	**EBI Chip Select** LT168 provides External Bus Interface (EBI) to drive MCU type display panel. This signal is the chip select of External Bus Interface (EBI).
EBI_RS	35	53	**EBI Register Select** This signal is the register select of EBI.
EBI_RD#	33	51	**EBI Data Read Control** This signal is the data read control signal of EBI.
EBI_WR#	34	52	**EBI Data Write Control** This signal is the data write control signal of EBI.
EBI_D[15:8]	25, 26, 27, 28, 29, 30, 31, 32	35, 36, 37, 38, 39, 40, 41, 42	**EBI High Byte Data Bus** These data signals are drive to MCU type display panel.
EBI_D[7:0]	-	43, 44, 45, 46, 47, 48, 49, 50	**EBI Low Byte Data Bus** These data signals are available for LT168B only, and are used to drive MCU type display panel.
Universal Serial Bus Module Signals (USB)			
DP	1	1	**USB Data Positive** This signal is used by the USB module.
DM	2	2	**USB Data Negative** This signal is used by the USB module.

Pin Name	Pin Number		Pin Description
	LT168A	LT168B	
I2C Module Signals			
SCL	-	56	**I2C Clock** This signal can be configured as the I2C clock line signal, or be configured as GPIO.
SDA	-	55	**I2C Data** This signal can be configured as the I2C data line signal, or be configured as GPIO.
Quad Serial Peripheral Interface Module 0 (QSPI0) The QSPI0 are used for embedded Flash. These signals are connected to internal QSPI Flash's pins directly.			
QSIO0[3:0]	-	-	**QSPI0 Master Input/Out** These signals are the serial data output or input from the QSPI0 in master mode.
QSCS0#	-	-	**QSPI0 Master Chip Select Output** This signal is the chip select signal from the QSPI0 in master mode and low active.
QSCK0	-	-	**QSPI0 Master Serial Clock Output** This signal is the serial clock output from the QSPI0 in master mode
Quad Serial Peripheral Interface Module 1 (QSPI1)			
QSIO1[3:0]	42, 41, 40, 39	62, 61, 60, 59	**QSPI1 Master Input/Out** These signals are the serial data output or input from the QSPI1 in master mode.
QSCS1#	38	58	**QSPI1 Master Chip Select Output** This signal is the chip select signal from the QSPI1 in master mode and low active.
QSCK1	43	63	**QSPI1 Master Serial Clock Output** This signal is the serial clock output from the QSPI1 in master mode
Quad Serial Peripheral Interface Module 2 (QSPI2)			
QSIO2[3:0]	13, 12, 11, -	22, 20, 19, 18	**QSPI2 Master Input/Out** These signals are the serial data output or input from the QSPI2 in master mode. These signals can also be configured as PWM1[1], PWM1[0], PWM0[3], PWM0[2] when not configured as QSPI2.
QSCS2#	-	16	**QSPI2 Master Chip Select Output** This signal is the chip select signal from the QSPI2 in master mode and low active. This signal can also be configured as PWM0[0] when not configured as QSPI2.

Pin Name	Pin Number		Pin Description
	LT168A	LT168B	
QSCK2	-	17	**QSPI2 Master Serial Clock Output** This signal is the serial clock output from the QSPI2 in master mode. This signal can also be configured as PWM0[1] when not configured as QSPI2.
Edge Port 0 Signals			
INT0[7:0]	9, 8, 7, 6, -, -, -, -	13, 11, 9, 7, 12, 10, 8, 6	**Interrupt Input** These bidirectional signals can be configured as either external interrupt sources or GPIO. These signals can also be configured as AIN[7:0] when not configured as interrupt sources or GPIO.
Edge Port 1 Signals			
INT1[7:0]	24, -, 36, 33, -, 34, 35, 17	34, 26, 54, 51, -, 52, 53, 27	**Interrupt Input** These bidirectional signals can be configured as either external interrupt sources or GPIO.
Pulse Width Modulator 0 Signals			
PWM0[3:0]	11, -, -, -	19, 18, 17, 16	These signals can be configured as either PWM 0 output or GPIO.
Pulse Width Modulator 1 Signals			
PWM1[3:0]	15, 14, 13, 12	24, 23, 22, 20	These signals can be configured as either PWM 1 output or GPIO.
Analog-to-Digital Converter Signals			
AIN[7:0]	9, 8, 7, 6, -, -, -, -	13, 11, 9, 7, 12, 10, 8, 6	**Analog Input** These analog signals can be configured as ADC analog channels. These signals can also be configured as INT0[7:0] when not configured as analog input.
Programming Debug Signals			
PGMCK	44	64	**Test Clock** This input signal is the test clock used to synchronize the Programming debug logic.
PGMIO	37	57	**Test Data Input/Output** This input/output signal is the serial input/output for testing instructions and data.
Clock Signals			
EXTAL	47	67	**Fast Oscillator Pad Input** The signal is the input of fast Oscillator Pad.
XTAL	48	68	**Fast Oscillator Pad Output** The signal is the output fast Oscillator pad.
OSC32K_XI	5	5	**32.768Khz Oscillator Pad Input** The signal is the input of **32.768Khz** Oscillator pad.
OSC32K_XO	4	4	**32.768Khz Oscillator Pad Output** The signal is the output **32.768Khz** Oscillator pad.

Pin Name	Pin Number		Pin Description
	LT168A	LT168B	
CLKOUT	17	27	**Clock Out** This output signal reflects the internal system clock. This signal can also be configured as INT1[0] when not configured as Clock output.
Reset Signals			
RESET#	16	25	**Reset In** This active-low input signal is used as the external reset request. The reset signal will place the CPU in supervisor mode with default settings for all register bits except for the register bits that can only be reset by POR. 0 = External Reset Assert 1 = External Reset Desert
RSTOUT	-	26	**Reset Out** This active-low output signal indicates that the internal reset controller has reset the chip. 0 = Chip is at reset status 1 = Chip is not at reset status This signal can also be configured as INT1[6] when not configured as Reset output.
Power and Ground Signals These signals provide system power and ground to the chip. Multiple signals are provided for adequate current capability. All power supply signals must have adequate bypass capacitance for high-frequency noise suppression.			
VDD33	45	21, 65	**3.3V Power** This signal supplies 3.3V positive power to the I/O pads and LDO.
VDD12	46	66	**1.2V LDO Output** This 1.2V LDO output signal is used to supply the power of the core logic. 1uF ceramic bypass capacitor is required to externally connect between the pad and VSS.
AVDD	10	14	This signal supplies 3.3V positive power to Analog module.
VBAT	3	3	This signal supplies battery power to RTC module.
VSS	49(1)	69 (1)	This signal supplies 3.3V negative supply (ground) to the I/O pads and LDO.
AVSS	-	15	This signal supplies 3.3V negative supply (ground) to the Analog Module.

Note (1) : This is the thermal pad and must be grounded directly to VSS or GND. When doing PCB layout, you need to pay attention to the soldering surface design of the pad. Please refer to Section 7.3 for details.

2.5. LT168A vs. LT168B

Table 2-3: LT168x Comparison

Function		LT168A	LT168B
Items	**Description**		
TFT LCD Panel	RGB Interface	--	V (480*480 max)
	16bit 8080 Interface	--	V (800*480 max)
	8bit 8080 Interface	V (480*320 max)	V (480*320 max)
	QSPI Panel	--	V
MCU Core & Memory	Core	32-bits RISC	32-bits RISC
	Speed	200MHz	200MHz
	Flash Capacity	512KB	2MB
	SRAM Capacity	256KB	256KB
	Display RAM(*1)	512KB	512KB
	External PSRAM	--	V
Other Interface	Uart Port	V (x3)	V (x3)
	SPI I/F	V (x1)	--
	QSPI I/F	V (x1)	V (x2)
	USB 2.0	V	V
	SD Card	V	V
	PWM Output	V (x5)	V (x8)
	Can Bus	V (x1)	V (x1)
	ADC Input	V (x4)	V (x8)
	RTP I/F	V	V
	CTP I2C I/F	V	V
	GPIO	V (x10)	V (x19)
	RTC	V	V
Appliaction and Upgrade	UI_Editor-II	V	V
	UI_Emulator-II	V	V
	USB Port Upgrade	V	V
	Uart Port Upgrade	V	V
	SD Card Upgrade	V	V
	Support 2nd Develop	V	V
Power and Package	Power	3.3V	3.3V
	Package	QFN-48	QFN-68

Note (1) : The Display RAM can be used as the normal SRAM, which means the maximum normal SRAM is up to 768KB.

3. Hardware Interface

3.1. Host Communication Interface

LT168 is designed to communicate with the Host MCU through UART interface. Please refer to UI_Editor-II user manual for communication protocol and related settings.

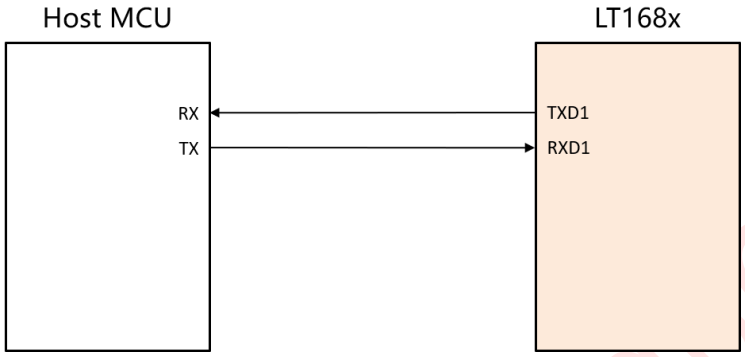


Figure 3-1: UART Connection between LT168x and Host MCU

3.2. TFT LCD Panel Interface

LT168 provides an External Bus Interface (EBI) to drive TFT panels with parallel 8080 interface. The data bus of this parallel interface is either 8 bits or 16 bits. LT168B can drive both 8bits/16bits parallel MCU panels, whereas LT168A can drive 8bits parallel MCU panels only. The reference connections are as shown in Figure 3-2 and 3-3. Using this interface TFT panel, LT168B can support a resolution of up to 800x480.

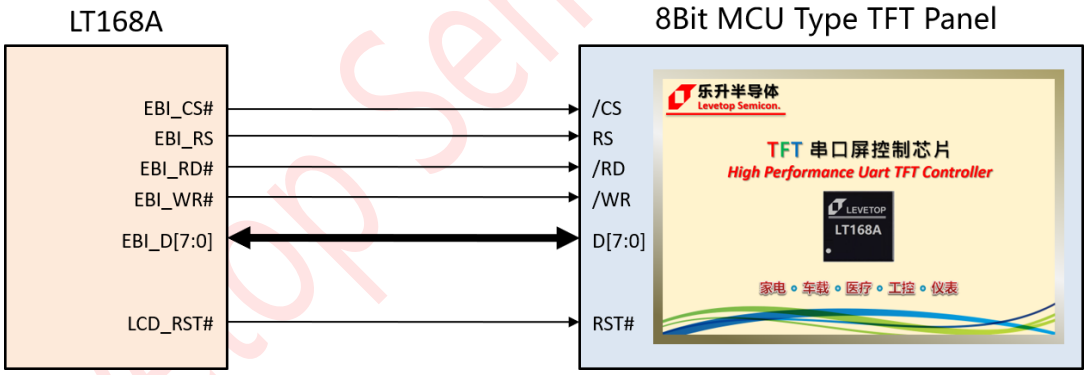


Figure 3-2: LT168A Connect to 8-bits MCU Panel

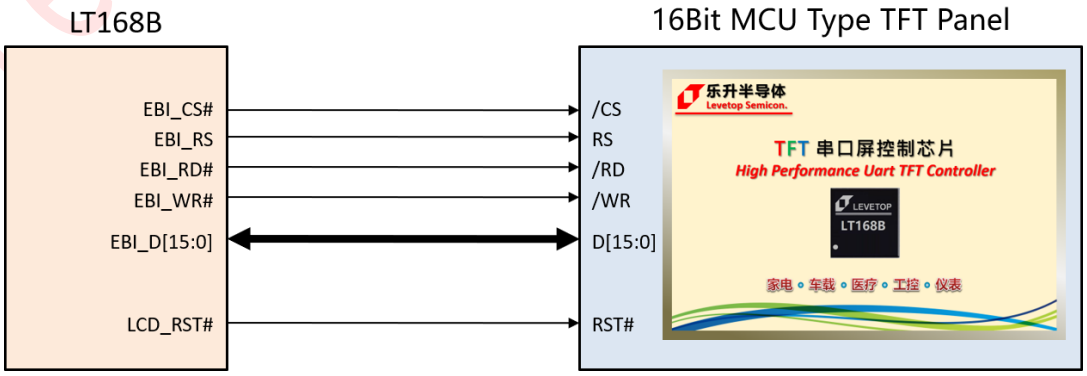


Figure 3-3: LT168B Connect to 16-bits MCU Panel

The LT168B is also available in RGB LCD interface mode. The reference schematic is shown in the figure below. The external PSRAM in the figure is reserved for display RAM data scratch area. If you want to achieve richer display effects such as image overlay, you can choose to add an external PSRAM chip. **Note:** LT168B supports RGB panels with maximum 480*480 resolution.

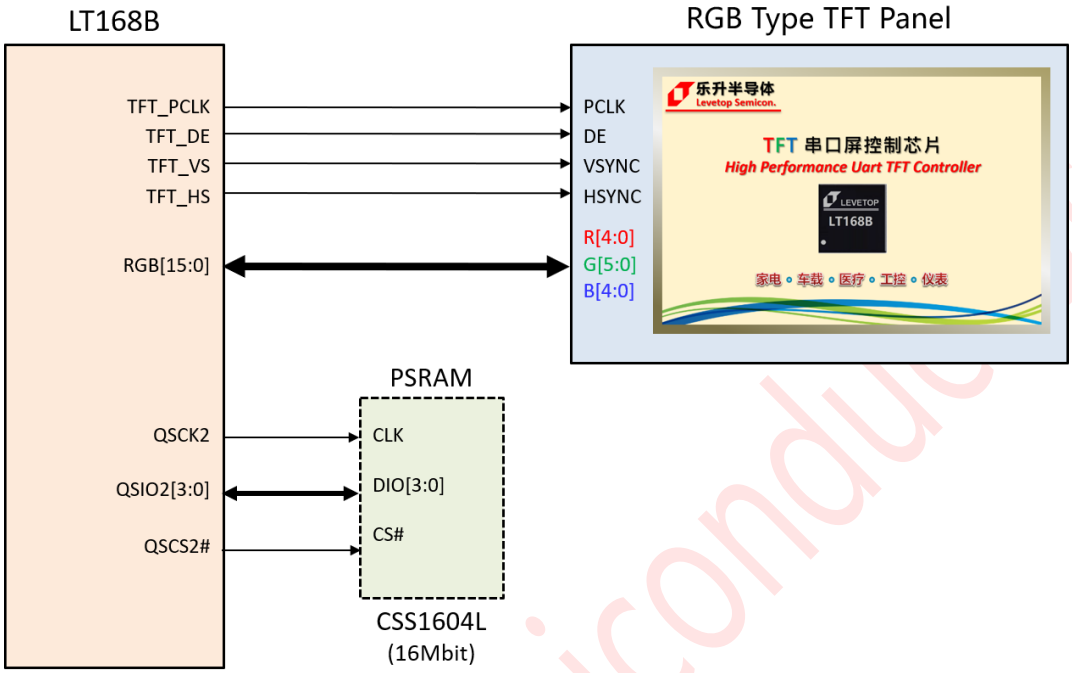


Figure 3-4: LT168B Connect to RGB Type TFT Panel

Table 3-1: The differences of LT168B for RGB Panel with or without PSRAM

Resolution	**RGB 480 x 272**		**RGB 480 x 480**		**8/16bit MCU 800 x 480**	
Functions	Without PSRAM	With PSRAM	Without PSRAM	With PSRAM	Without PSRAM	With PSRAM
Page buffer refresh	Support	Support	Not Support	Support	Not Support	Support
The size of the limit display by PNG overlay	480 x 272	480 x 272	200 x 200	480 x 480	320 x 320	800 x 480
Display page ZIP compression	Not Support	Support	Not Support	Support	Not Support	Not Support
Display page sliding	Not Support	Support	Not Support	Support	Not Support	Not Support

There is also a kind of TFT panel with QSPI interface on the TFT panel market. This kind of panel needs the display chip to provide high-speed QSPI signal and constantly refresh the display data in order to achieve good use effect. The LT168B also supports this kind of TFT display. The reference circuit diagram is as follows:

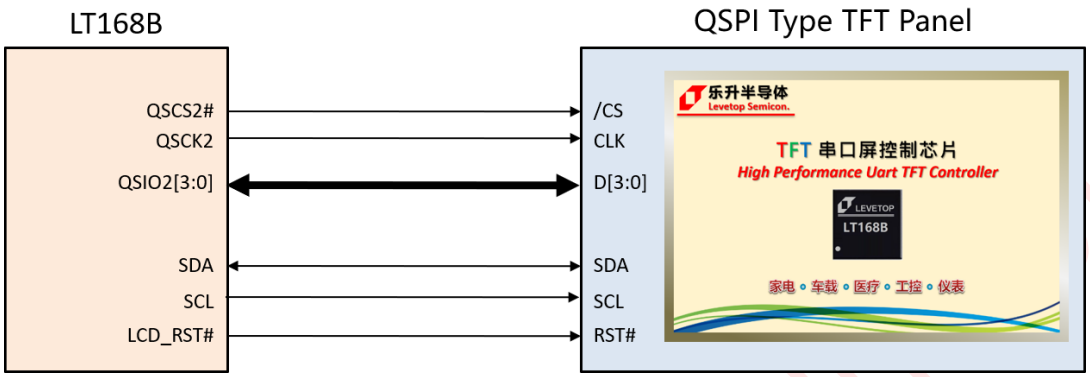


Figure 3-5: LT168B Connect to QSPI Type TFT Panel

3.3. QSPI Flash Interface

LT168 has two sets of QSPI interfaces, and one is for connecting to an external QSPI Flash. The external Flash is used to store images, animations, fonts and other information. Host MCU can send commands to request LT168 to retrieve the data from the QSPI Flash and transmit the data onto the connected TFT panel for display. The image data can be programmed to the external SPI Flash by several means. Please refer to UI_Editor-II user manual for more detail. Another set of QSPI interface can be used to connect to other QSPI devices. See Section 3.12 SPI/Uart Interface for more detail.

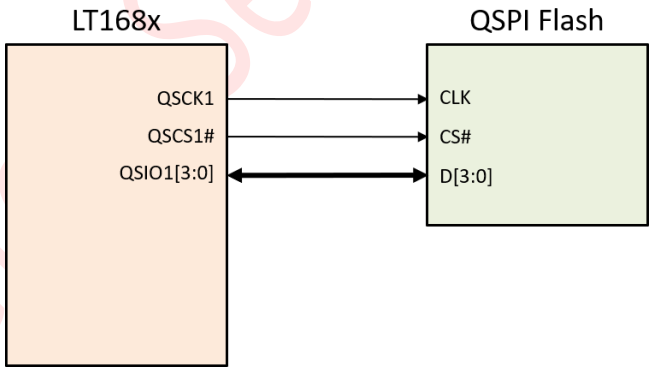


Figure 3-6: LT168x Connect to QSPI Flash

3.4. Touch Panel Interface

LT168 has an ADC analog input and I2C interface that can be used to interface directly to resistive or capacitive touch panel. Upon receiving the touch information, LT168 will process it and transmit it to the Host MCU. The reference schematics are as followings:

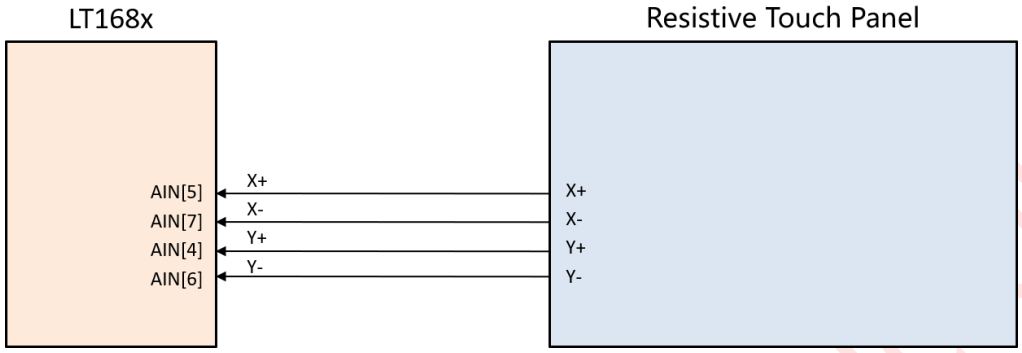


Figure 3-7: LT168x Connect to Resistive Touch Panel

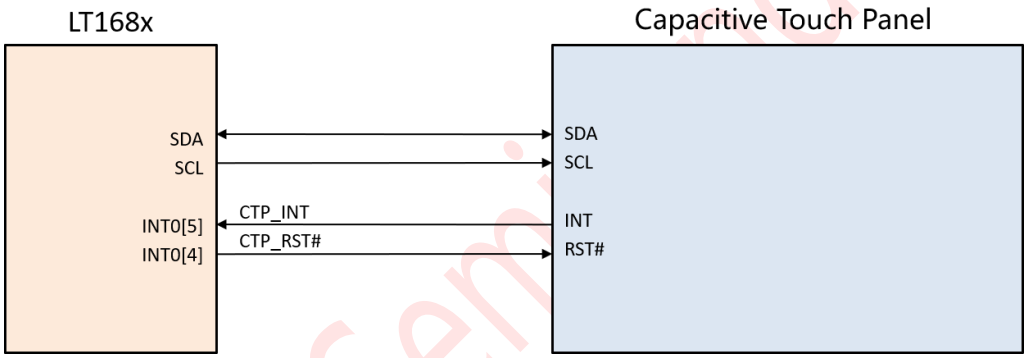


Figure 3-8: LT168x Connect to Capacitive Touch Panel

3.5. Clock Interface

LT168x needs an external 12MHz Crystal Oscillator as the internal PLL and USB module clock source.

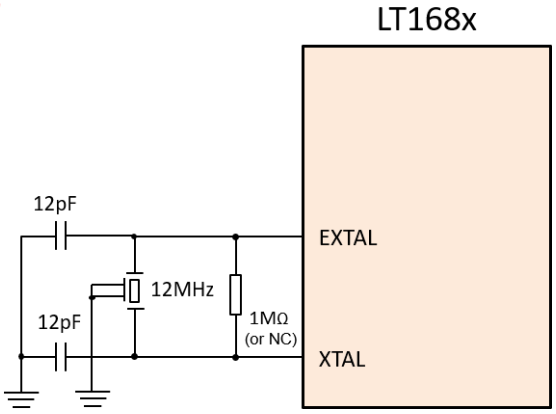


Figure 3-9: External Clock Circuit

3.6. Backlight Control Circuit

LT168 uses PWM1[3] to provide a backlight control signal - "BL_PWM" that can be used to control TFT LCD panel backlight. The reference schematics are as followings:

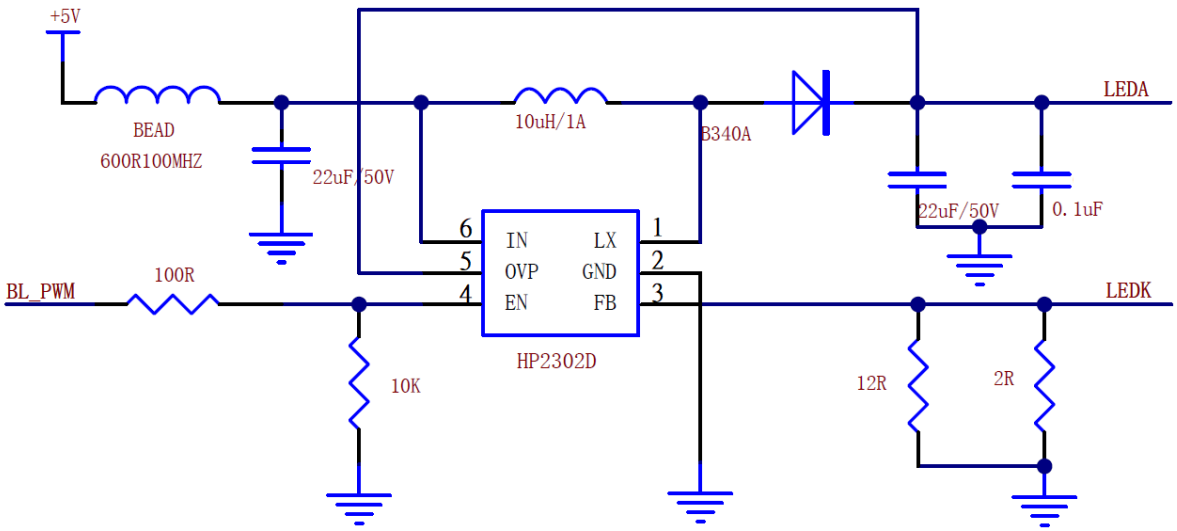


Figure 3-10: TFT LCD Backlight Circuit Example 1

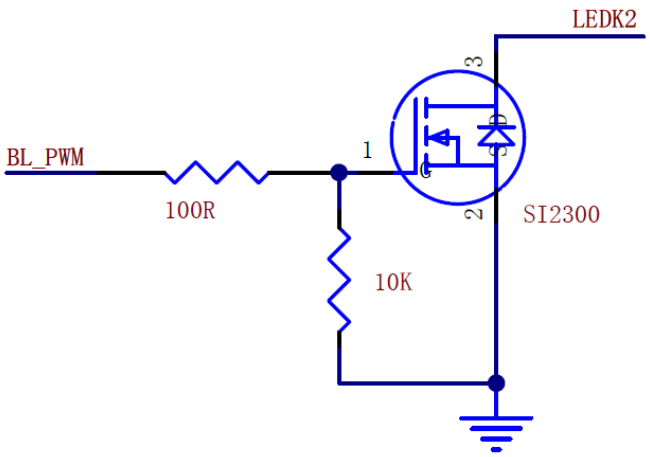


Figure 3-11: TFT LCD Backlight Circuit Example 2

3.7. Can Bus Interface

LT168 provides a CAN Bus interface. The reference schematic is as following:

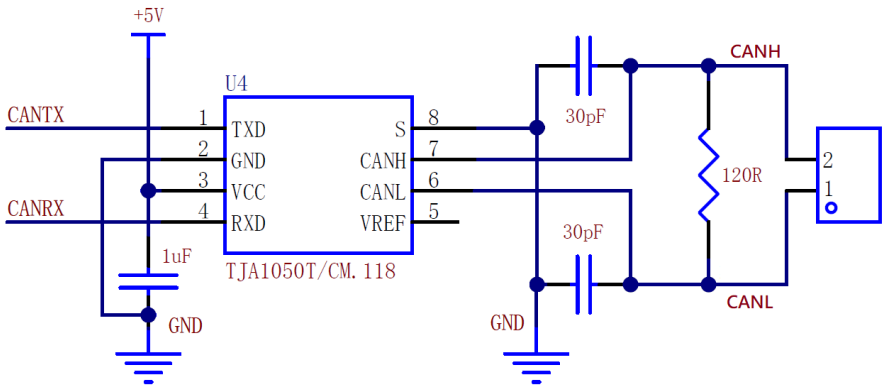


Figure 3-12: Canbus Circuit Example

3.8. Audio Interface

LT168 uses PWM1[2] to provide an analog sound output signal - "HORN", which can be used as a sound playback or to push a buzzer. The reference schematic is as following:

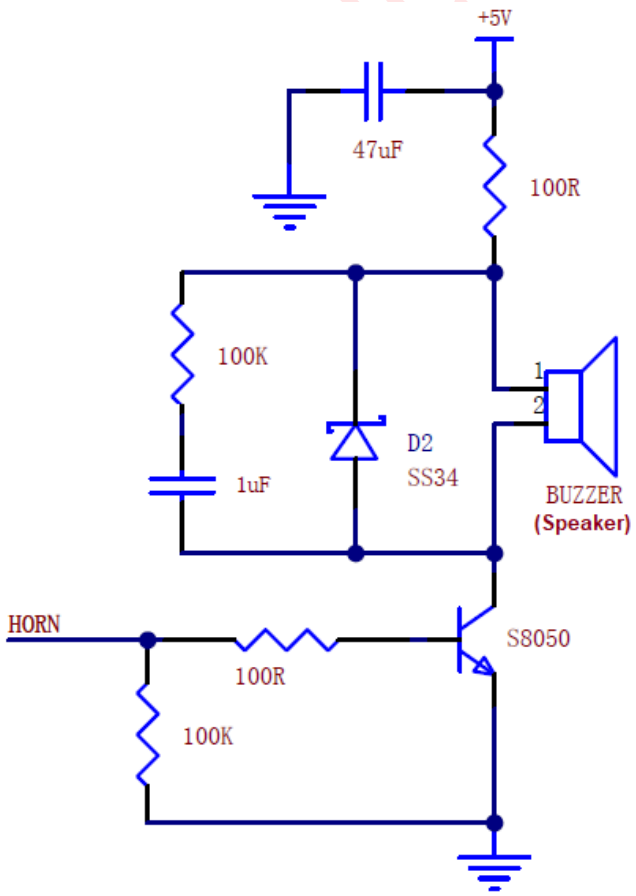


Figure 3-13: Audio Output Application Circuit

3.9. Real Time Clock Circuit

LT168 contains RTC (Real Time Clock) inside. To utilize the RTC, a 32.768KHz crystal circuit must be provided. The reference schematic is as following:

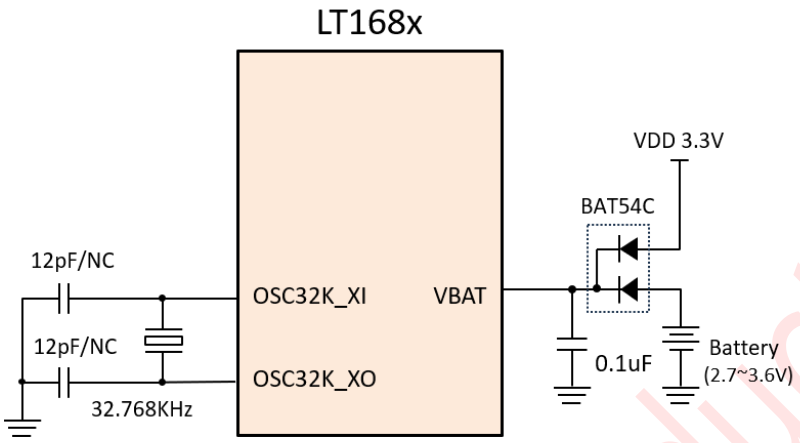


Figure 3-14: RTC Application Circuit

3.10. Reset Interface

There are two hardware reset sources for LT168, both of which are synchronized by the internal clock:

– Power on Reset

– External Reset Pin (RESET#)

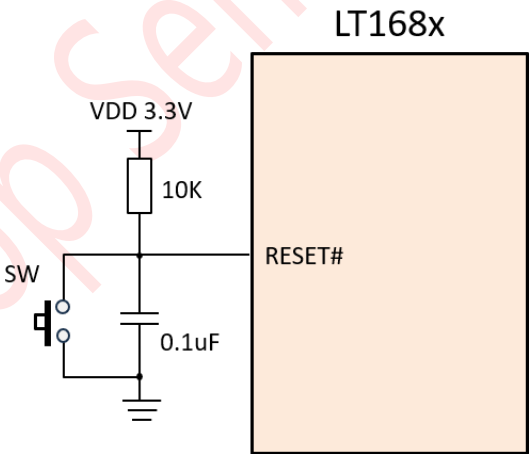


Figure 3-15: External Reset Circuit

To avoid internal reset instability caused by power fluctuations in industrial applications or battery powered environments, it is recommended to add a dedicated reset chip circuit (as shown in the following figure):

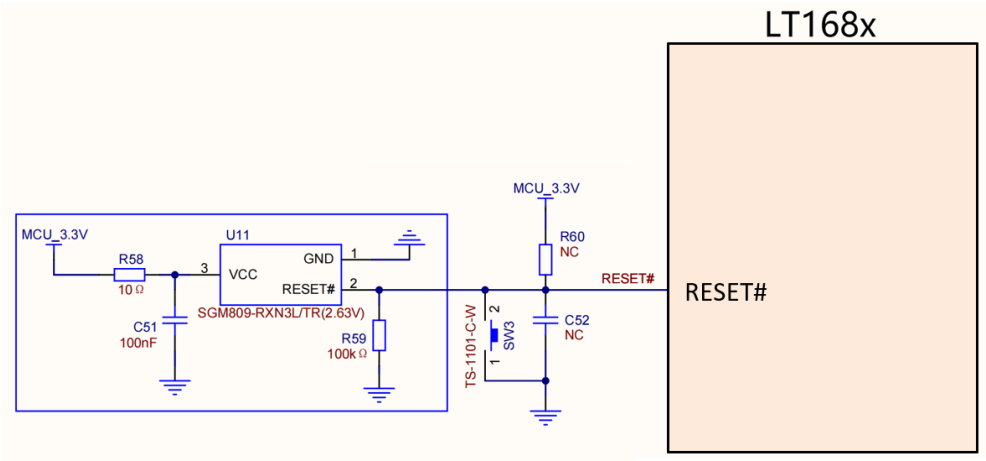


Figure 3-16: Add Dedicated Reset Chip Reference Circuit

3.11. USB Interface

LT168 provides a USB interface with USB Slave functionality. This USB interface can be used to connect with a PC for updating the internal MCU program of LT168, and the data of the external SPI Flash. Please refer to UI_Editor-II user manual for more detail.

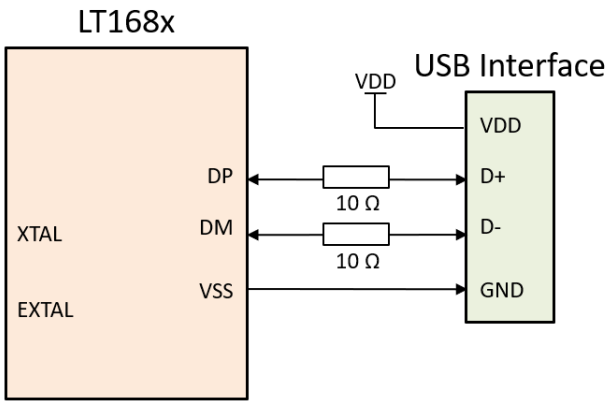


Figure 3-17: LT168x Connect to USB Connector

3.12. SPI/Uart Interface

In addition to the necessary pins for the TFT panel, LT168x also provides some pins for external SPI/QSPI components. If QSPI2 is connected to QSPI PSRAM (Pseudo SRAM), it can be used to temporarily store display image materials or data, which is convenient for the MCU to perform image overlay and a large amount of data processing. The rest of the Uart interfaces for connecting to devices shuch as WiFi module, Bluetooth module, etc. The reference schematic is as following:

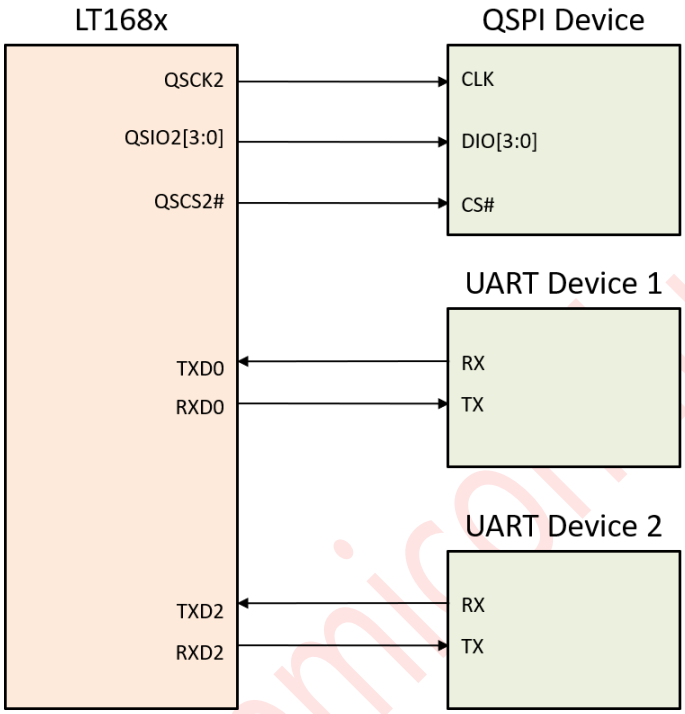


Figure 3-18: Extension for SPI and Uart Device

4. System Memory Map

4.1. Introduction

The embedded memory and address map of LT168 are listed below:

- Up to 128M Bytes of External SPI/QSPI Flash Memory
- 512K Bytes or 2M Bytes of Internal QSPI Flash Memory
- 8K Bytes of Internal Boot ROM Memory
- 768K Bytes of Internal Static Random-Access Memory (SRAM)
  – System RAM: the Upper 256K Bytes and Address Range from 0x00800000
  – Display RAM: the Lower 512K Bytes and Address Range from 0x00840000
- Internal Memory Mapped Registers

4.2. Address Map

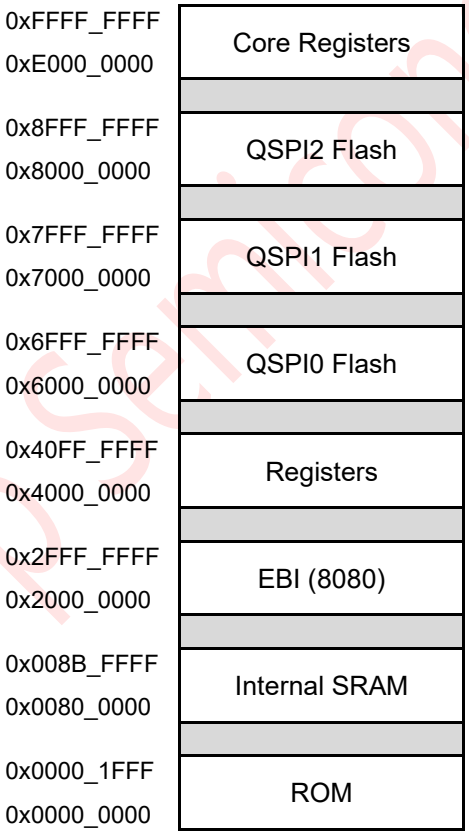


Figure 4-1: Address Map

The LT168's Register Map and SPI's Address Map are show as following table:

Table 4-1: Register Address Location Map

Base Address	Maximum Size	Usage Module
0x4000_0000	64Kbyte	Direct Memory Access Controller (DMAC)
0x4001_0000	64Kbyte	Chip Configuration Module (CCM)
0x4002_0000	64Kbyte	Reset Control Module (RCM)
0x4003_0000	64Kbyte	Clock and Power Control Module (CLKPWRM)
0x4004_0000	64Kbyte	Programmable Interrupt Timer 0 (PIT0)
0x4005_0000	64Kbyte	Programmable Interrupt Timer 1 (PIT1)
0x4006_0000	64Kbyte	Programmable Interrupt Timer 2 (PIT2)
0x4007_0000	64Kbyte	Programmable Interrupt Timer 3 (PIT3)
0x4008_0000	64Kbyte	Serial Communication Interface 1 (SCI1)
0x4009_0000	64Kbyte	Serial Communication Interface 0 (SCI0)
0x400A_0000	64Kbyte	Analog Comparator 0 (COMP0)
0x400B_0000	64Kbyte	Analog Comparator 1 (COMP1)
0x400C_0000	64Kbyte	Serial Communication Interface 2 (SCI2)
0x400D_0000	64Kbyte	Pulse Width Modulator 0 (PWM0)
0x400E_0000	64Kbyte	Pulse Width Modulator 1 (PWM1)
0x400F_0000	64Kbyte	Edge Port Module 0 (EPORT0)
0x4010_0000	64Kbyte	Edge Port Module 1 (EPORT1)
0x4011_0000	64Kbyte	Analog-to-Digital Convertor (ADC)
0x4012_0000	64Kbyte	Efuse Control Module (EFM) and Option Byte (OPB)
0x4013_0000	64Kbyte	WatchDog Timer (WDT)
0x4014_0000	64Kbyte	Real Time Controller (RTC)
0x4015_0000	64Kbyte	Inter-Integrated Circuit (I2C)
0x4016_0000	64Kbyte	USB2.0 Full-Speed Device Controller (USBC)
0x4017_0000	64Kbyte	Crossbar Switch (XBAR)
0x4018_0000	64Kbyte	External Bus Interface (EBI)
0x4019_0000	64Kbyte	CACHE Module (CACHEM)
0x401A_0000	64Kbyte	RGB Controller (RGBC)
0x401B_0000	64Kbyte	Blender Controller (BLDC)
0x401C_0000	64Kbyte	CANBus Controller (CANBC)
0x401D_0000	64Kbyte	Edge Port Module 2 (EPORT2)
0x6000_0000	64Kbyte	Synchronous Serial Interface 0 (SSI0) - QSPI0
0x7000_0000	64Kbyte	Synchronous Serial Interface 1 (SSI1) - QSPI1
0x8000_0000	64Kbyte	Synchronous Serial Interface 2 (SSI2) - QSPI2
0xE000_0000	4Kbyte	Embedded Interrupt Controller (EIC)
0xE000_1000	4Kbyte	Embedded Programmable Timer (EPT)

Note:

See module sections for details of how much of each block is being decoded. Accessing to addresses outside the module memory maps(and also the reserved area 0x00CB_0000 ~ 0x00CF_FFFF will not be responded to and will result in a bus monitor transfer error exception.

5. Electrical Characteristic

This chapter provides the electrical characteristic parameters and limits for LT168.

5.1. Absolute Maximum Ratings

Table 5-1: Absolute Maximum Rating

Symbol	Item	Range	Unit
V_{DD33}	Power Supply	-0.5 ~ 4.6	V
V_{IN}	Input Voltage Range	-0.5 ~ VDD33+0.5	V
V_{OUT}	Output Voltage Range	-0.5 ~ VDD33+0.5	V
P_D	Power Dissipation	≦300	mW
T_{OPR}	Operation Temperature	-40 ~ 105	℃
T_{ST}	Storage Temperature	-55 ~ 150	℃
T_{SOL}	Soldering Temperature	260	℃

If the loading to the chip exceeds the absolute maximum rating listed in **Table 5-1**, it may result in permanent damage to the chip. Although the chip contains circuitry to resist damage from high quiescent voltages, do not apply more voltages on the chip than the values rated in the table. These values are only ratings and do not mean that the chip functions properly under these conditions.

5.2. DC Electrical Specification

Table 5-2: IO Static Characteristic (3.3V)

Item	Symbol	Min	Typical	Max	Unit
IO Supply Power	VDD33	2.97	3.3	3.63	V
Input High Voltage	V_{IH}	2.0	-	VDD33+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Output High Voltage	V_{OH}	2.4	-	VDD33	V
Output Low Voltage	V_{OL}	0	-	0.4	V
Input Leakage Current	I_{IN}	-	-	1	uA
Pull-Up Resistor	RPU	33	41	62	KΩ
Pull-Down Resistor	RPD	33	42	68	KΩ

Table 5-3: Power Characteristic

Item	Symbol	Min	Typical	Max	Unit
Chip Power	VDD33	2.97	3.3	3.63	V
ADC Power I/P	AVDD	2.97	3.3	3.63	V
Chip Core Power (LDO O/P)	VDD12	1.1	1.2	1.3	V
RTC Power	VBAT	2.7	3.3	3.6	V

5.3. Electrostatic Discharge (ESD) Protection

Table 5-4: Electrostatic Discharge Protection Characteristic

ESD Test	Symbol	Max	Unit	Reference Standard
Human Body Model	HBM	4000	V	ANSI/ESDA/JEDEC JS-001-2017
Machine Model	MM	200	V	JEDEC JESD22-A115C-2010
Charged Device Model	CDM	800	V	ANSI/ESDA/JEDEC JS-002-2022
Latch Up	LU	200	mA	JEDEC JESD78F.01-2022, @105℃

Note: When performing manual soldering, it is recommended that personnel and equipment should be treated with anti-static. For example, appropriate temperature and humidity environment, grounding of welding equipment, anti-static workbench, and welding personnel wearing anti-static wrist straps, etc.

5.4. VDD Power Up Timing

When using the LT168x, it is important to pay attention to the power up requirements of VDD. The VDD33 must maintain a waiting time of at least 400ms at the low voltage (V_L) at the time of power-up (T_{WAIT}). At the same time, the rise time (T_R) of VDD33 from V_L to normal operating voltage should not be too long. The normal operating voltage range must be reached within 500ms. Otherwise, the MCU inside the LT168 will not boot properly.

Table 5-5: VDD Power Up Characteristic

Item	Symbol	Description	Min.	Nom.	Max.	Unit
Rise Time	T_R	The rise time of input voltage from V_L to the normal operating voltage	-	-	500	ms
Wait Time	T_{WAIT}	The retention time of the V_L before Power On	400	-	-	ms
VDD Input Voltage	V_L	at $T=T_1$ on pin VDD33 (The input voltage before Power Up)	-	-	200	mV
VDD Input Voltage	V_H	Normal Operation Voltage	2.97	3.3	3.63	V

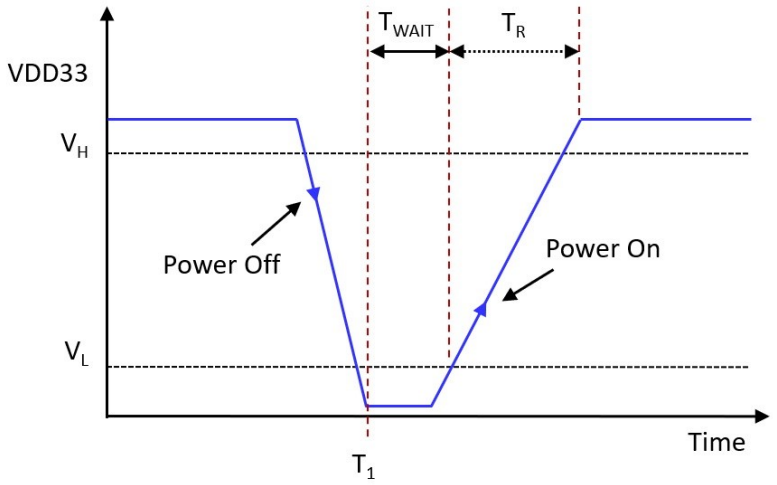


Figure 5-1: VDD Power up Timing Requirement

6. Application Circuit

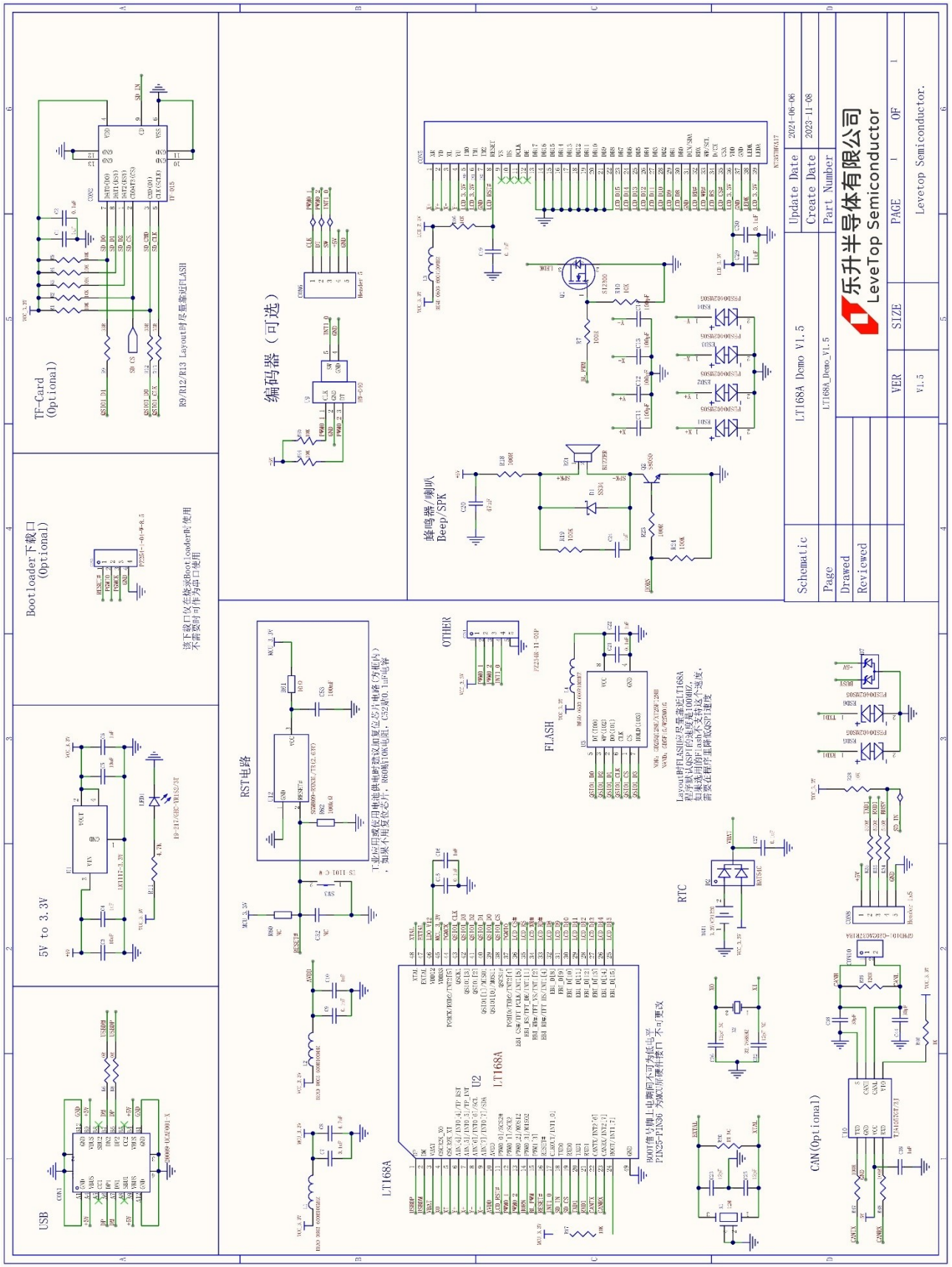


Figure 6-1: LT168A for 8bit MCU Panel Application Circuit

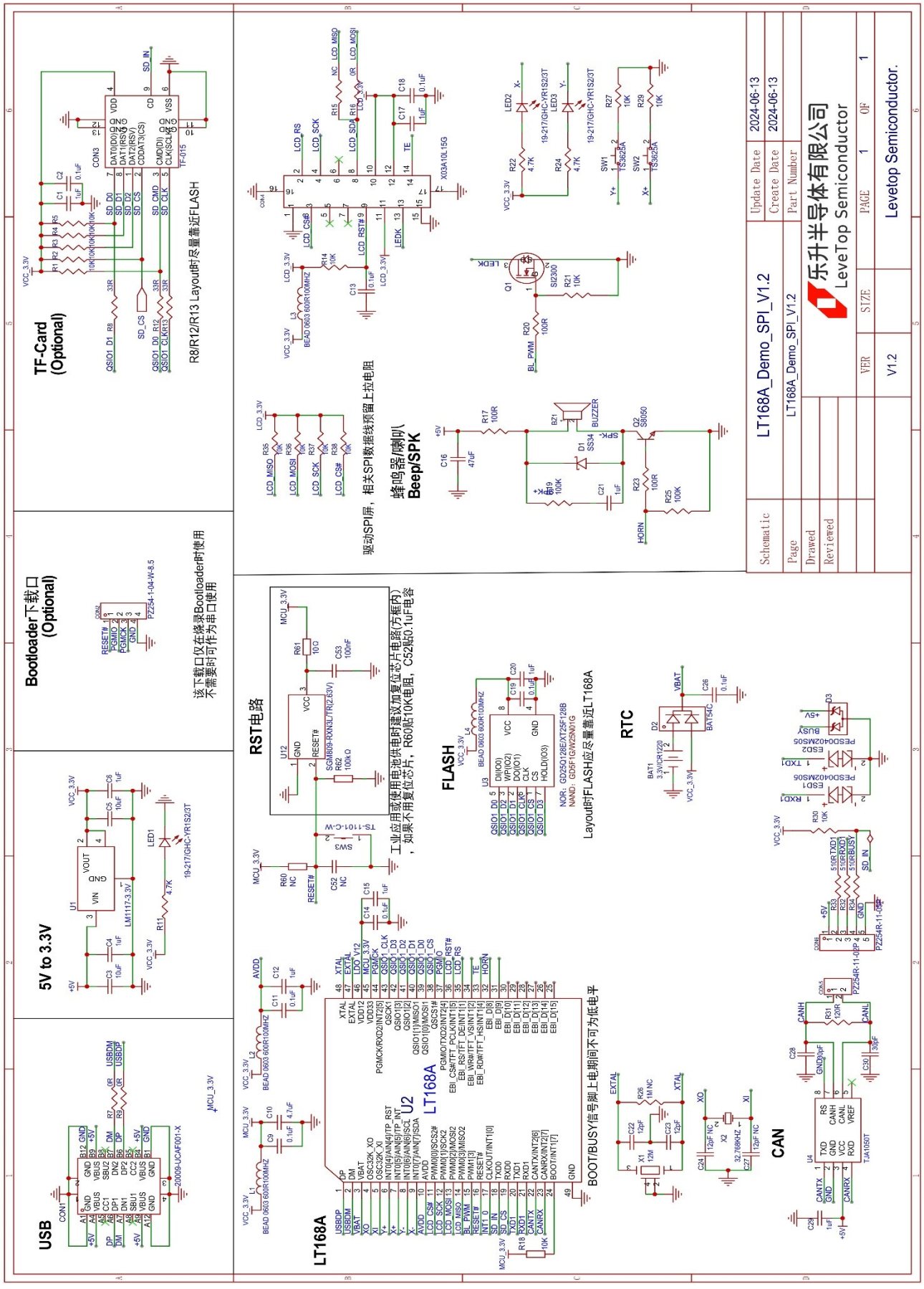


Figure 6-2: LT168A for SPI Panel Application Circuit

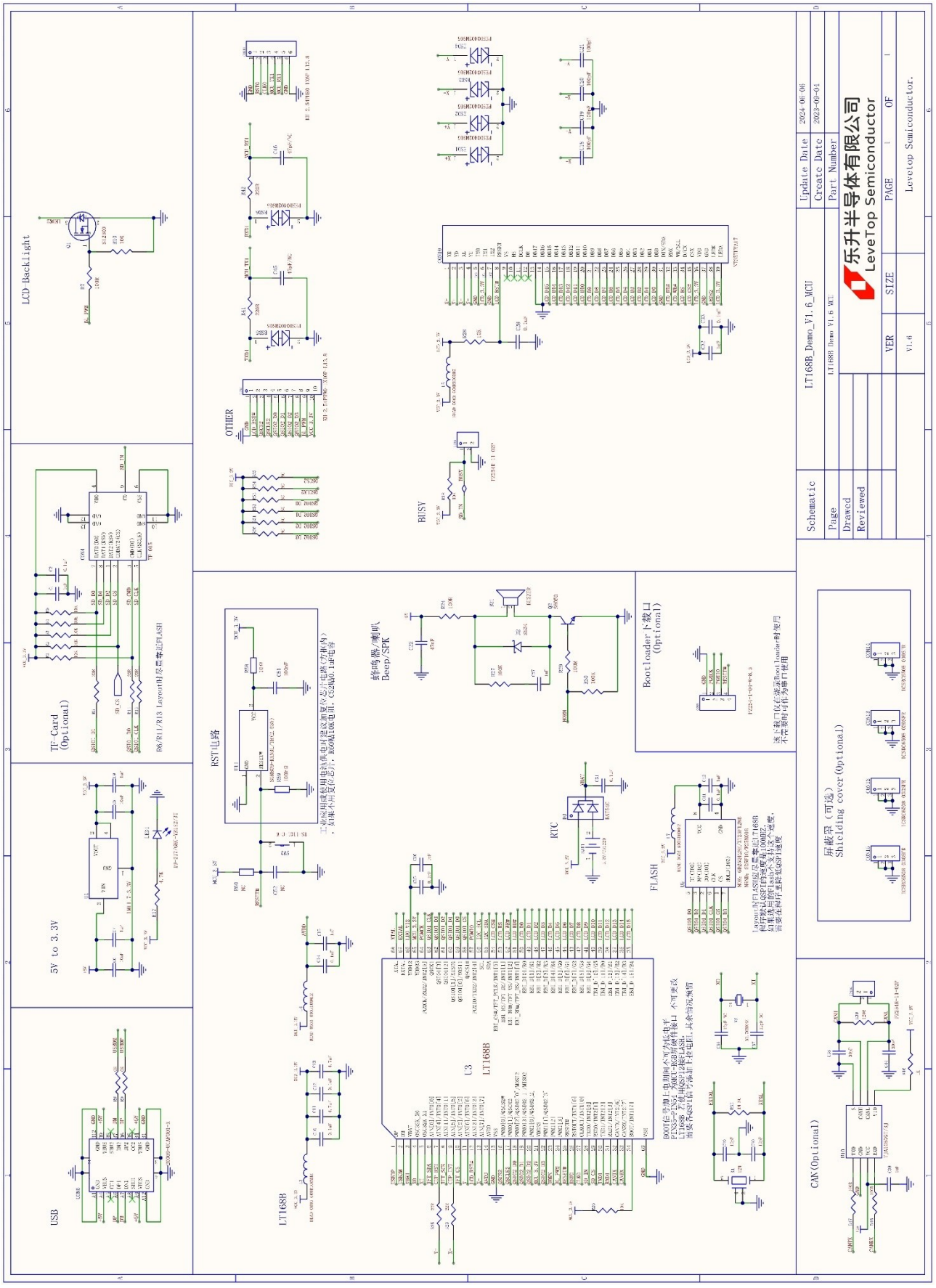


Figure 6-3: LT168B for 16bit MCU Panel Application Circuit

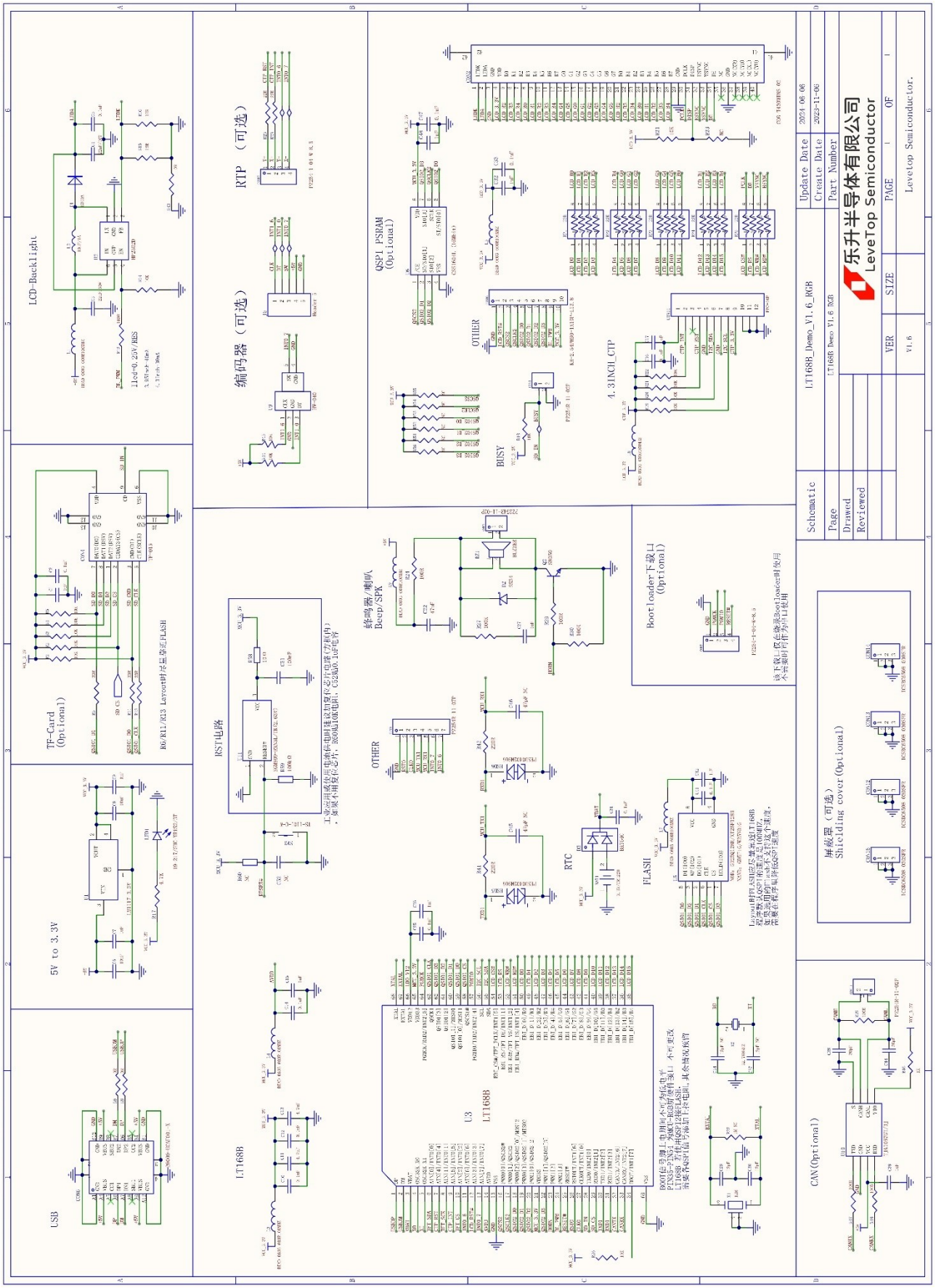


Figure 6-4: LT168B For RGB Panel Application Circuit

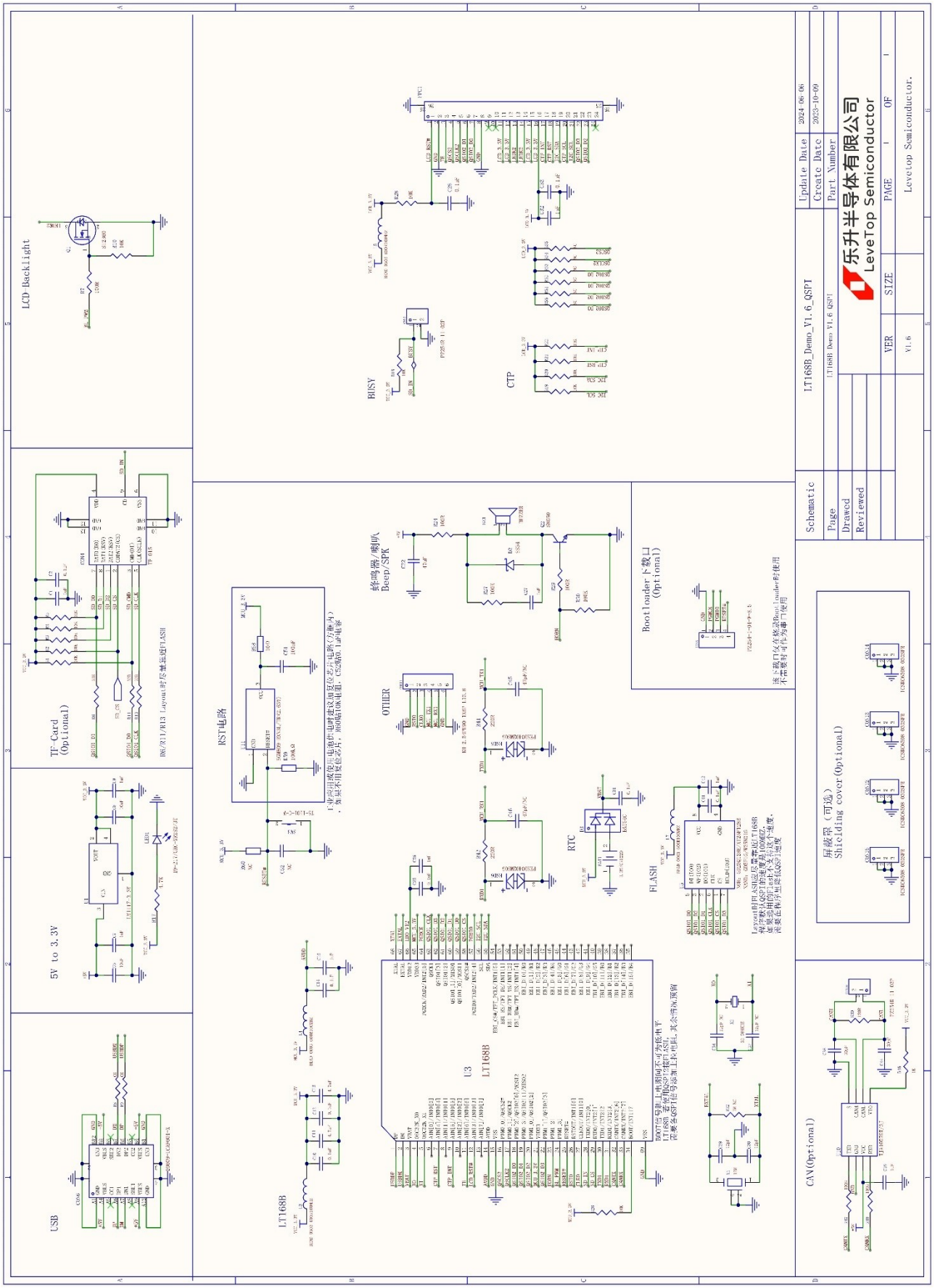


Figure 6-5: LT168B for QSPI Panel Application Circuit

7. Package Information

7.1. LT168A (QFN-48pin)

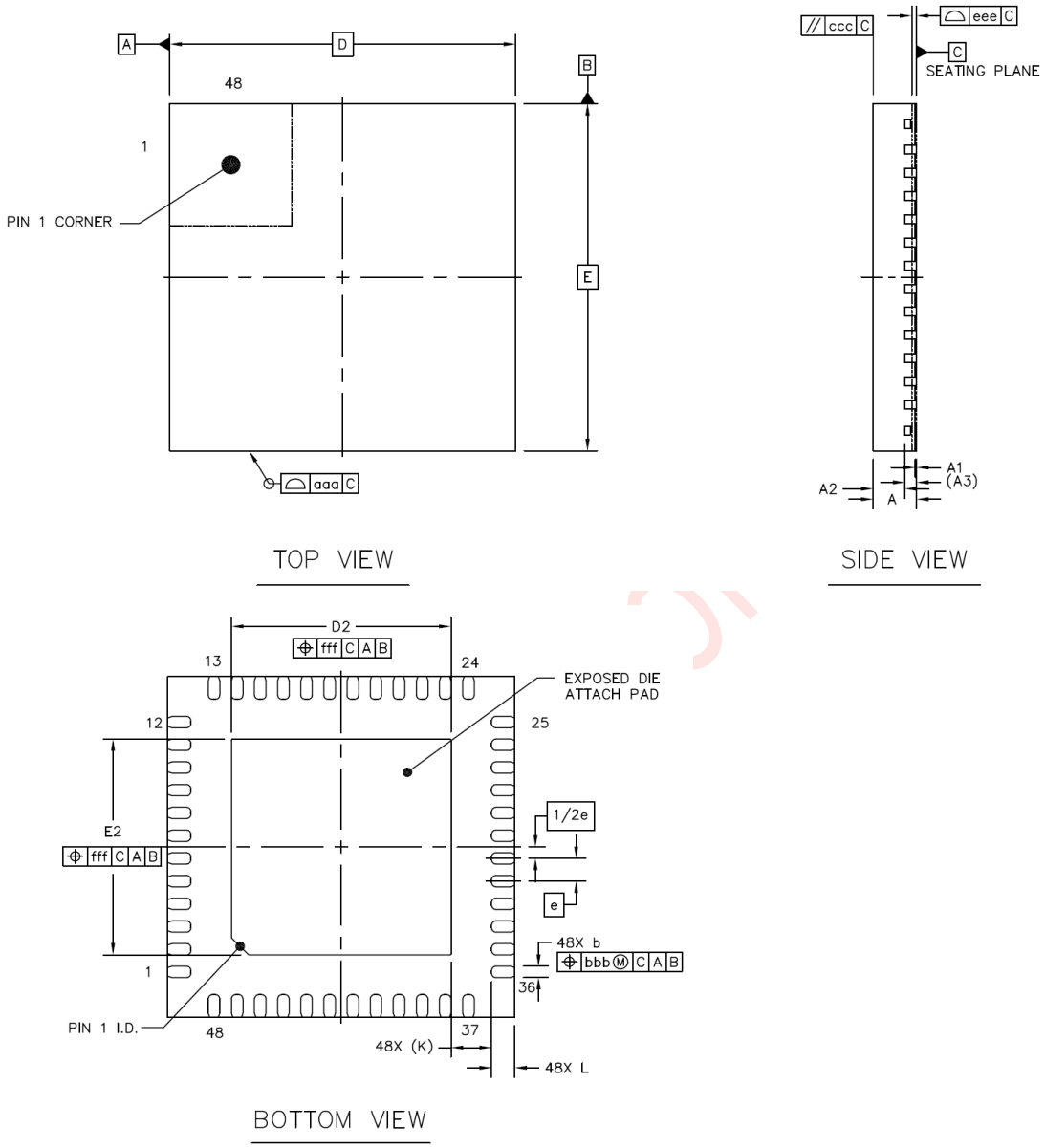


Figure 7-1: LT168A Package Overview

Table 7-1: LT168A Package Parameter

		Symbol	Min.	Nom.	Max.
Total Thickness		A	0.80	0.85	0.90
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	--	0.55	--
L/F Thickness		A3		0.203 Ref	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		6 BSC	
	Y	E		6 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	D2	3.7	3.8	3.9
	Y	E2	3.7	3.8	3.9
Lead Length		L	0.3	0.4	0.5
Lead Tip to Exposed Pad Edge		K		0.7 Ref	
Package Edge Tolerance		aaa		0.1	
Mold Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Lead Offset		bbb		0.07	
Exposed Pad Offset		fff		0.1	

Note: When layout PCB, LT168A Thermal Pad Zone must be connected to ground.

7.2. LT168B (QFN-68pin)

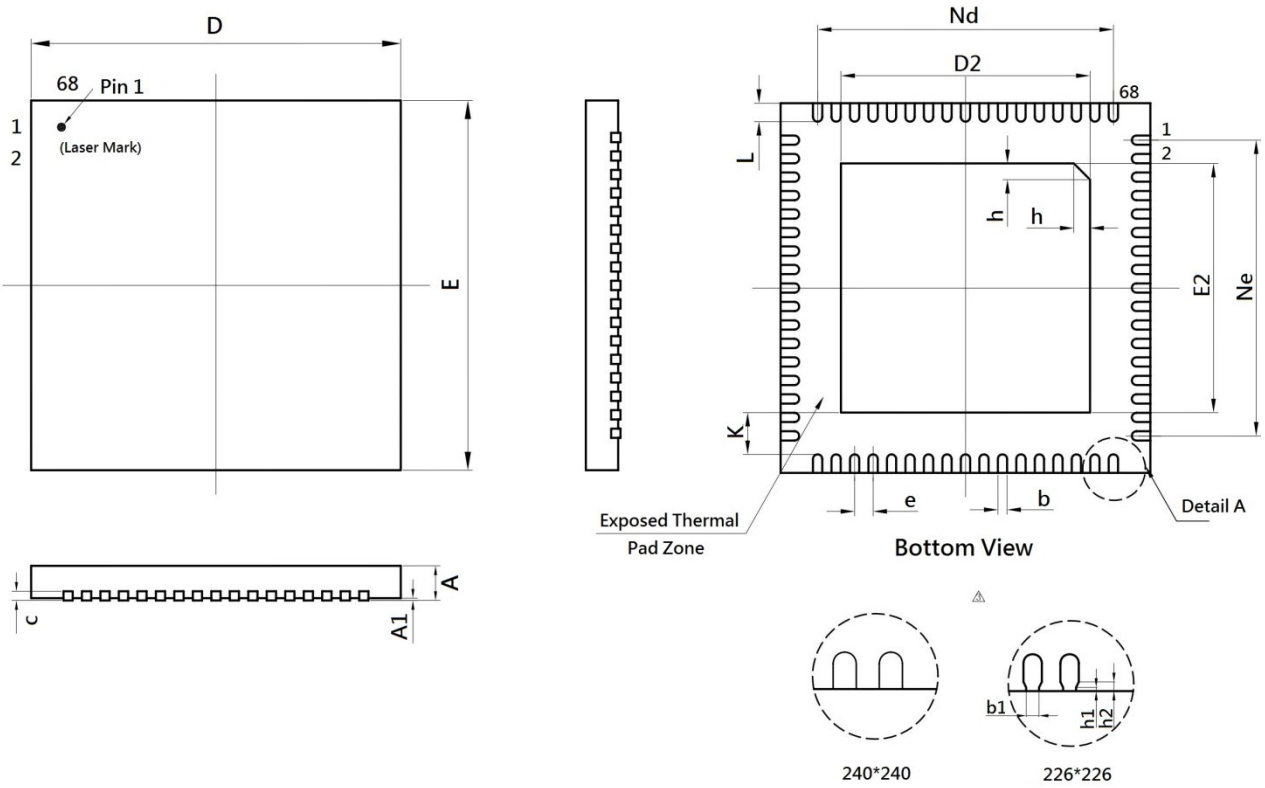


Figure 7-2: LT168B Package Overview

Note: When layout PCB, LT168B Thermal Pad Zone must be connected to ground. Please refer to Section 7.3 for PCB routing of ground thermal pad.

Table 7-2: LT168B Package Parameter

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	0.80	0.85	0.90	Ne	6.40BSC		
A1	-	0.02	0.05	L	0.35	0.40	0.45
b	0.15	0.20	0.25	K	0.20	-	-
b1	0.14REF			h	0.30	0.35	0.40
c	0.18	0.20	0.25	h1	0.04REF		
D	7.90	8.00	8.10	h2	0.10REF		
e	0.40BSC			D2	5.39	5.49	5.59
Nd	6.40BSC			E2	5.39	5.49	5.59
E	7.9	8.0	8.10				

7.3. PCB Design for Ground Pad

The LT168 is available in a QFN package with a ground (GND) thermal pad on the back of the chip. In order to achieve better heat dissipation and reduce the risk of soldering, it is recommended to divide the copper surface of the PCB on the bottom pad of LT168 into four or more small solder surfaces (square or round) when laying out the PCB. And the spacing between each soldering surface is set at ~0.8mm, so as to avoid incomplete soldering caused by the PCB using a complete soldering surface that is the same or even larger than the size of the LT168 pad, or the chip deformation and poor contact caused by the pulling of the PCB and the chip pad after soldering cooling.

The correct PCB pad layout is shown in the following two LT168B examples, the light yellow area in the middle is the ground pad at the bottom of the LT168, and the gray area is the small PCB ground pad (solder surface). Each pad has 1~2 vias grounded.

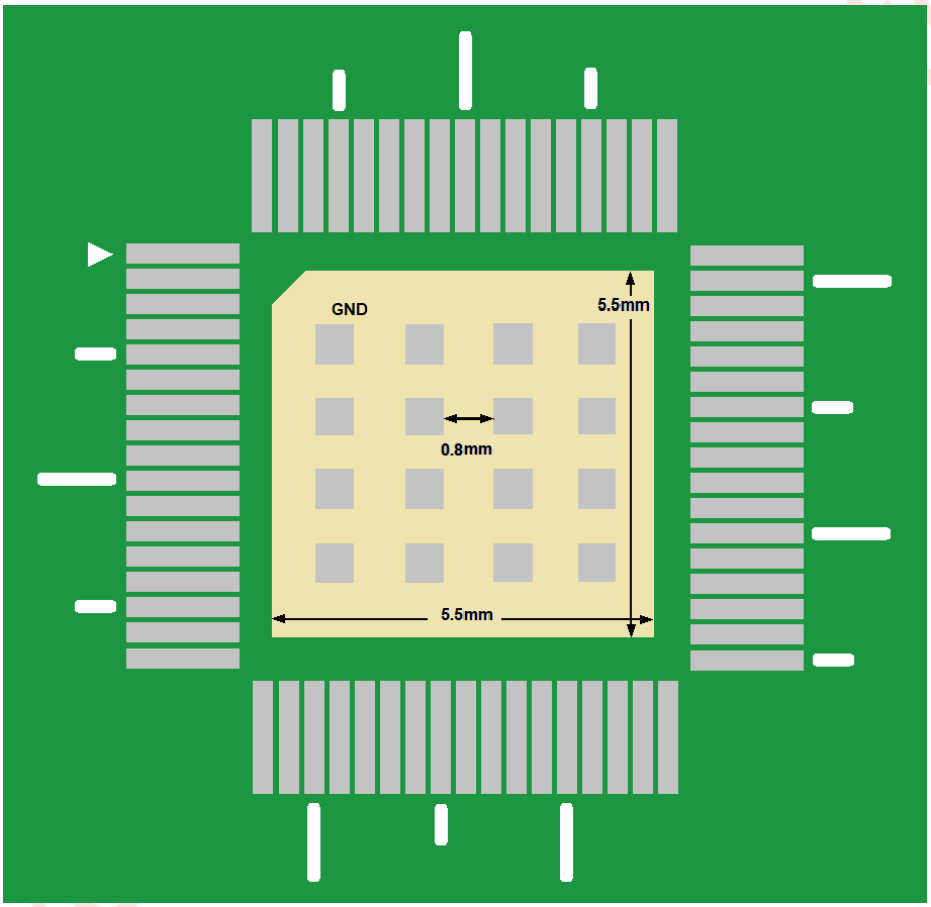


Figure 7-3: PCB Design Recommendation for the LT168B Bottom Ground Pad (1)

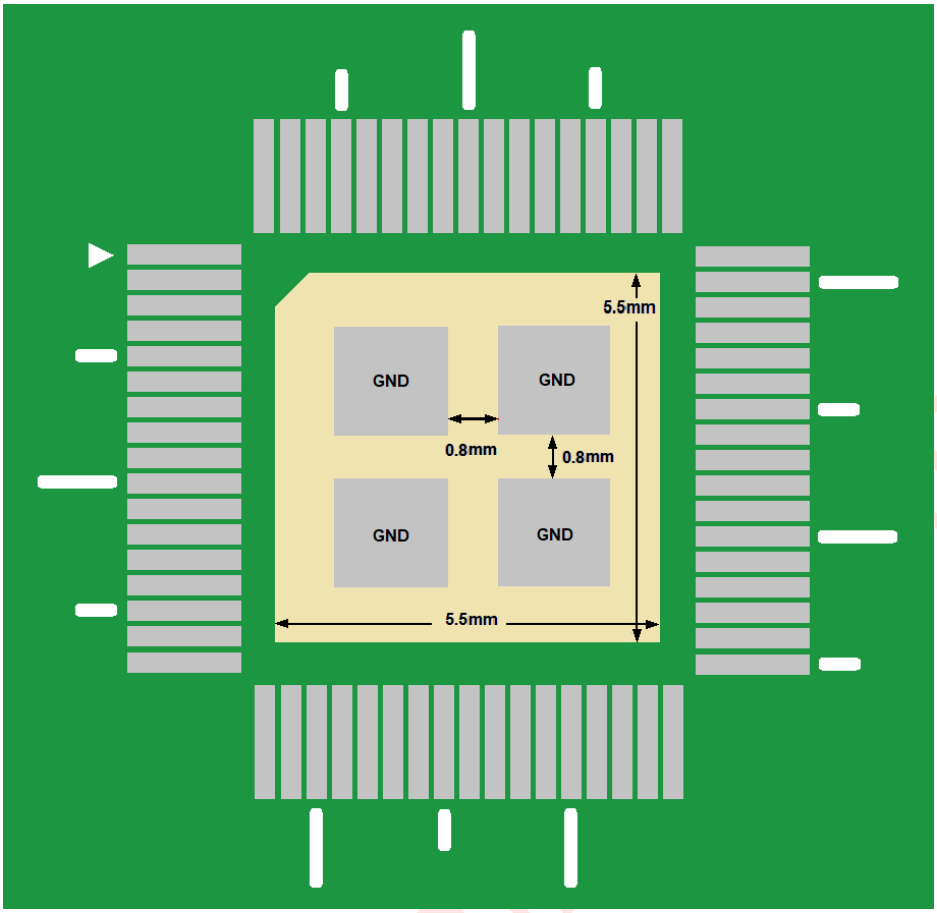


Figure 7-4: PCB Design Recommendation for the LT168B Bottom Ground Pad (2)