乐升半导体
LEVETOP

LT165

Uart TFT LCD Display Controller

Brief Specification

V1.2

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Version History

Version	Date	Description
V1.0	2025/07/08	● Priliminary Release
V1.0A	2025/08/27	● Schematic Modification: Serial port upgrade UART0 Change to use UART1； added reservation RTP (Resistive Touch Panel) circuit
V1.1	2025/09/16	● Update LT165B Information.
V1.2	2025/12/24	● UpdateTable 5-2: IO Static Characteristic ● Update Table 5-3: Power Characteristic

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1. LT165 Introduction

1.1. Introduction

LT165 is a series of low-cost and high-performance Uart serial panel control chips, which embedded a 32bit RISC core architecture internally The main function of this chip is to provide Uart serial communication, allowing the main control MCU to easily transmit the content to be displayed on the TFT panel to the driver on the TFT panel through simple communication commands. The internal hardware and serial program of LT165 provide high-speed image processing capabilities, which can achieve excellent display efficiency and reduce the time required for the main control MCU to process graphic displays. LT165 supports 8bit parallel TFT panel with a resolution of 320 * 240 or TFT LCD panel with SPI serial ports.

The internal frequency of LT165 can reach 150MHz and contains 32KB SRAM. In addition to providing serial communication, it also provides a QSPI Flash interface for quickly reading program code, images, animations, and other information stored in external SPI Flash LT165 can be used in conjunction with the serial panel development software (UI-Editor) and simulation software (UI-Eimulator) developed by Levetop Semiconductor to directly develop the UI display interface of the product on the PC computer. The display functions it supports include image display, GIF animation display, loop image display, progress bar display, display, text string display, PWM (DMA mode) audio playback, and multi variable control display combined with touch function In addition to improving display efficiency, it also significantly shortens the development cycle of TFT LCD displays. In addition, LT165 also provides 2 sets of SCI (Uart) interfaces that can be connected to Bluetooth modules or WiFi modules, as well as CanBus, analog input AIN, PWM, INT interrupt interfaces, and capacitive touch input interfaces. These interfaces can also be used as general purpose IO interfaces and come with an RTC clock. The functions of this chip increase the practicality and applicability of the serial port TFT LCD panel, and the chip characteristics also comply with automotive standard design and application. LT165 can support dual panel display or parallel panel display applications, with good smoothness of deisplay and extremely high cost-effectiveness.

On many small electronic products, LT165 can also use internal resources as the main control MCU, and the main control and TFT display functions can be completed by one LT165. Its display function is very suitable for use in electronic products with low resolution TFT-LCD panels, such as replacing original monochrome panel products, or increasing product texture and grade, without causing too much loading on the original MCU of the product's main control terminal. It can be applied to various small electronic products such as smart home appliances, handheld control devices, industrial control boards, electronic instruments, testing equipment, small electric motorcycles, personal medical aesthetics, small testing equipment, charging equipment, water and electricity meters, smart speakers with TFT LCD panel, robot eyes and other products.

The LT165 has two different package models, as shown below:

Table 1-1: LT165 Models

Type	Package	SRAM	TFT Panel
LT165A	QFN-40	32KB	● 8bits 8080 I/F TFT Panel ● SPI I/F TFT Panel

QFN-40 (5.0*5.0 mm²)

Figure 1-1: LT165A Package Overview

1.2. Internal Block Diagram

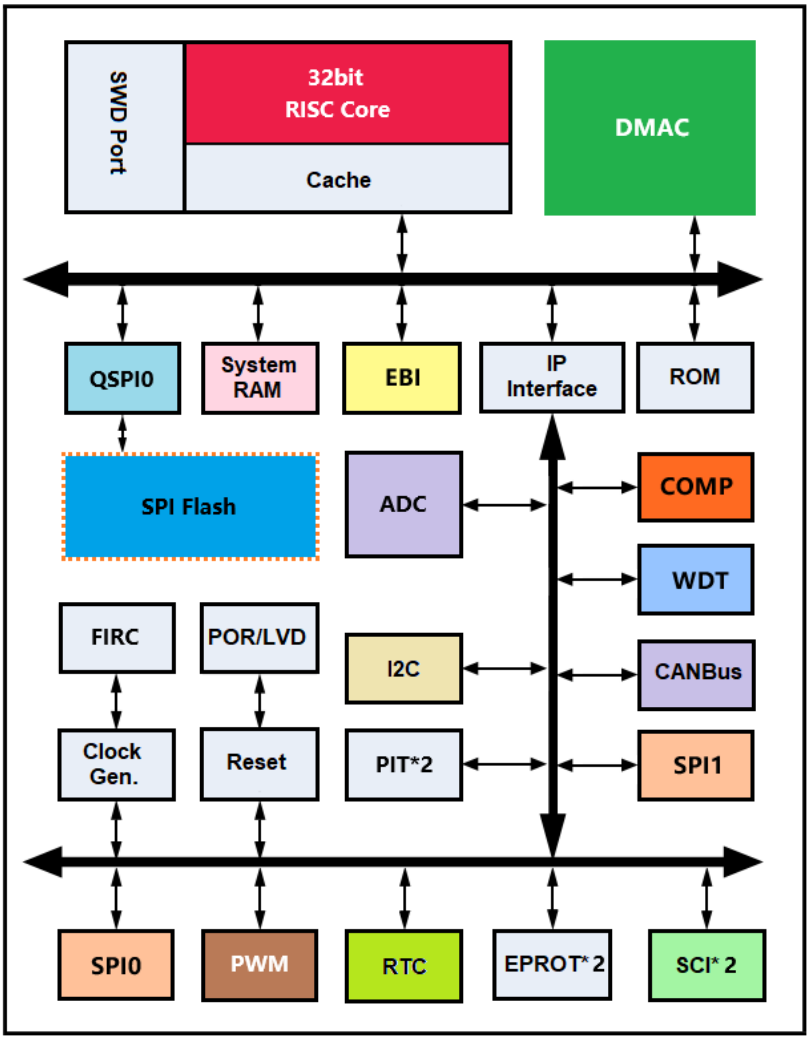

Figure 1-2: Internal Block Diagram

1.3. Features

1.3.1. 32bits RISC Core

- 32bit load/store reduced instruction set computer (RISC) architecture with fixed 16bit instruction length
- 16 entry 32bit general-purpose register file
- Efficient 3-stage execution pipeline, hidden from application software
- Single-cycle instruction execution for many Instructions, three cycles for branches
- Support for byte/halfword/word memory accesses
- Embedded interrupt controller, support nested vector interrupts.
- Single-cycle 32bit x 32bit hardware integer multiplier array
- 3~13 cycles hardware integer divider array

1.3.2. 32K Bytes SRAM

- Single cycle byte, half-word (16bit), and word (32bit) reads and writes
- Two segments for improving performance at certain application
  - System RAM0: 16Kbytes and address range from 0x0080_0000 to 0x0080_3FFF
  - System RAM1: 16Kbytes and address range from 0x0080_4000 to 0x0080_7FFF

1.3.3. 6K Bytes ROM

- Single cycle byte, half-word (16bit), and word (32bit) reads access

1.3.4. 2K Byte Cache

- 2-way set -associative organization
- Two AHB bus interfaces, a master and a slave interface

1.3.5. External Bus Interface (EBI)

- Programmable wait states -up to 256 wait states can be programmed before the access terminated
- One programmable asynchronous active-low chip selects.
- Programmable chip selects wait cycle
- To interface with various panels, up to 256 chip selects asserted cycle can be programmed.
- Programmable read/write asserted cycle
- Programmable read/write negated cycle
- Support 8bits port size.
- Support 8080 standard bus

1.3.6. DMA Module

- 16 programmable channels to support independent 8, 16 or 32bit single value or block transfers
- Support of variable sized queues and circular queues
- Source and destination address registers independently configured to post-incrementor remain constant
- Each transfer initiated by peripheral, CPU, periodic timer interrupt or DMA channel request
- Peripheral DMA request sources possible from QSPI, QADC
- Each DMA channel able to optionally send interrupt request to CPU on completion of single value or block transfer
- DMA transfers possible between system memories and all accessible memory mapped locations

including peripheral and registers

- DMA supports the following functionality:
  - Scatter Gather
  - Channel Linking
  - Inner Loop Offset
  - Arbitration
  - Fixed Group, fixed channel
  - Round Robin Group, fixed channel
  - Round Robin Group, Round Robin Channel
  - Fixed Group, Round Robin Channel
  - Channel preemption
  - Cancel channel transfer
- Interrupts – The DMA has a single interrupt request for each implemented channel and a combined DMA Error interrupt to flag transfer errors to the system

1.3.7. RESET Module

- Internal power on reset circuit
- Five sources of reset:
  - Power-on reset
  - External pin
  - Software reset
  - Watchdog timer
  - Program Voltage Detect Reset
- Status flag indicates source of last reset

1.3.8. Programmable Interrupt Timer (PIT)

- 16bit counter with modulus "initial count" register
- Selectable as free running or count down
- 16 selectable prescalers — 2^0 to 2^{15}
- support DMA interface

1.3.9. Watch Dog Timer (WDT)

- 16bit counter with modulus "initial count" register
- Pause option for low-power modes
- Up to 2000ms service time

1.3.10. Real Time Clock (RTC)

- Support loading time data to and read time data from seconds, minutes, hours and days counters
- Support alarm settings
- Interrupt sources:
  - second, minute, hour, day interrupts
  - programmable alarm interrupts
  - 1KHz/32KHz periodic interrupts

1.3.11. EPORT

- Eight Channels for each EPORT
- Rising/falling edge select
- Low/High level sensitive
- Interrupt pins configurable as general-purpose I/O

1.3.12. SPI Module

- Master mode and slave mode
- Wired-OR mode
- Slave-select output
- Mode fault error flag with central processor unit (CPU) interrupt capability
- Double-buffered operation
- Serial clock with programmable polarity and phase
- Control of SPI operation during doze mode
- Reduced drive control for lower power consumption

1.3.13. SSI / QSPI Module

- Serial-master operation
- DMA controller interface
- Enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
- Clock stretching support in enhanced SPI transfers
- Data item size (4 to 32bits) – Item size of each data transfer under control of the programmer
- Configurable depth of the transmit and receive FIFO buffers from 2 to 256 words deep. The FIFO width is fixed at 32bits
- Enhanced SPI support
- Execute in Place (XIP) mode support

1.3.14. SCI / UART Module

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13bit modulo divider) with configurable oversampling ratio from 4x to 256x
- Interrupt, polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
  - Receive data match
- Hardware parity generation and checking
- Programmable 8bit, 9bit or 10bit character length
- Programmable 1bit or 2bit stop bits
- Three receiver wakeup methods:
  - Idle line wakeup

  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13bit break character generation / 11bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  - Separate configurable watermark for receive and transmit requests
  - Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty

1.3.15. CANBus Controller

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 ~ 8 bytes data length
  - Programmable bit rate up to 1 Mbit/s
  - Content-related addressing
- 16 Message Buffers of zero to eight bytes data length
- Each MB configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Includes 288bytes (16 MBs) of SRAM used for MB storage
- Includes 64 bytes (16 MBs) of SRAM used for individual Rx Mask Registers
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8bits) IDs, with individual masking capability
- Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
- Unused MB and Rx Mask Register space can be used as general purpose SRAM space
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode
- Hardware cancellation on Tx message buffers

1.3.16. PWM Module

- Four channel each PWM controller
- Programmable period
- Programmable duty cycle
- Two Dead-Zone generator
- Capture function
- Pins can be configured as general-purpose I/O

1.3.17. ADC Module

- High performance
  - 12bit, 10bit, 8bit or 6bit configurable resolution
  - ADC conversion time: 1.0 μs for 12bit resolution (1 MHz), 0.88 μs conversion time for 10bit resolution, faster conversion times can be obtained by lowering resolution.
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support
- Low power
  - Application can reduce PLCK frequency for low power operation while still keeping optimum ADC performance. For example, 1.0 μs conversion time is kept, whatever the frequency of PCLK.
  - Wait mode: prevents ADC overrun in applications with low frequency PLCK
  - Auto off mode: ADC is automatically powered off except during the active conversion phase. This dramatically reduces the power consumption of the ADC.
- Analog input channels
  - 3 external analog inputs
  - 1 channel for internal temperature sensor
- Start-of-conversion can be initiated:
  - By software
  - By hardware triggers with configurable polarity
- Conversion modes
  - Can convert a single channel or can scan a sequence of channels. Single mode converts selected inputs once per trigger
  - Continuous mode converts selected inputs continuously
  - Discontinuous mode
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events.
- Analog watchdog
- Single-ended and differential-input configurations

➢ Converter uses an internal reference or an external reference

1.3.18. I2C Module

- Supports 7bit addressing.
- Supports Standard Mode, Fast Mode and High-Speed Mode
- Software option to select between High-Speed mode and Standard/Fast mode
- Compatibility with standard and fast-mode of I2C bus version 2.1 standard.
- Multiple-master operation.

- Software-programmable for one of 64 different serial clock frequencies.
- Software-selectable acknowledge bit.
- Interrupt-driven, byte-by-byte data transfer.
- Arbitration-lost interrupt with automatic mode switching from master to slave.
- Transfer completion and read configure interrupt.
- Start and stop signal generation/detection.
- Repeated START signal generation.LT32A05_SPEC_ENG/V0.0
- Acknowledge bit generation/detection.
- Bus-busy detection.
- Option slave address receiving enable when system clock stop mode
- SCL or SDA line gpio function supported

1.3.19. Analog Comparator

- Programmable response time
- Programmable hysteresis
- Support analog input multiplexer with nine selections
- Two optional outputs: filtered or asynchronous output
- Selectable rising/falling edge interrupt

1.3.20. Touch Sensor

- Support four touch keys
- Support three clock mode with charge or discharge function
  - Frequency range from 369KHz to 6MHz with Fixed clock divider
  - Frequency with PRS 1.5MHz follow Normal Distribution
  - Frequency with PRS 1.5MHz follow even Distribution
- Programmable counter clock frequency with 24/12/6/4MHz
- Programmable counter width range from 9 to 16bits
- Support synchronous scan mode

1.3.21. Power Management Unit (PMU)

- Support on-chip 1.2V LDO with maximum load current 150mA
- 1.2V LDO support two mode: lower power, high power

1.3.22. Voltage Detector

- Programmable voltage detector

1.3.23. Internal Oscillator

- 128KHz on-chip oscillator clock for watchdog and PMU
- Fast Internal RC clock which can be used for system clock

1.3.24. External Crystal Oscillator

- 32.768KHz external crystal Oscillator clock which can be used for RTC
- Fast external crystal Oscillator clock which can be used for system clock

1.4. System Block Diagram

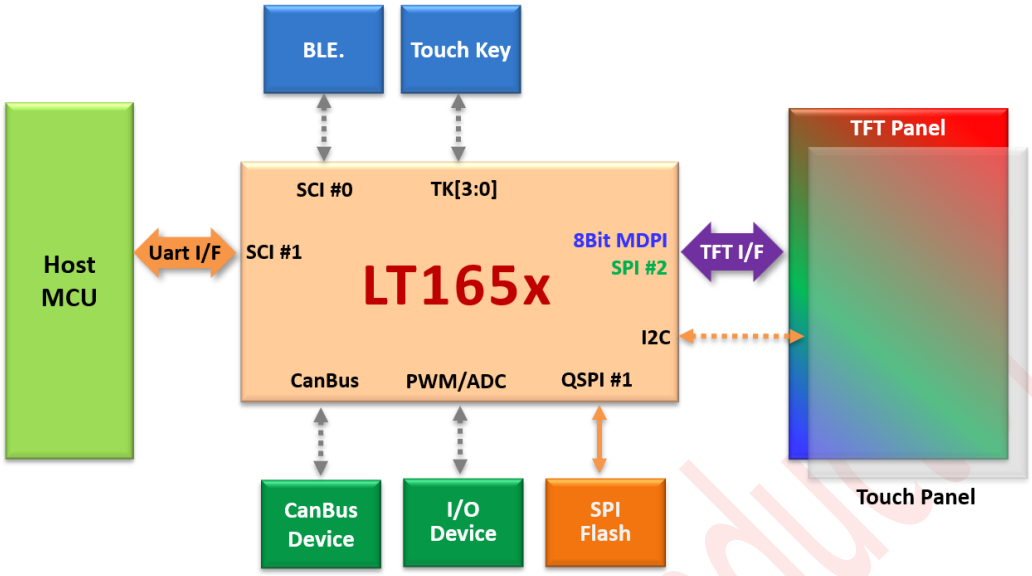

Figure 1-3: System Block of LT165

2. Signal Description

2.1. Pin Assignment

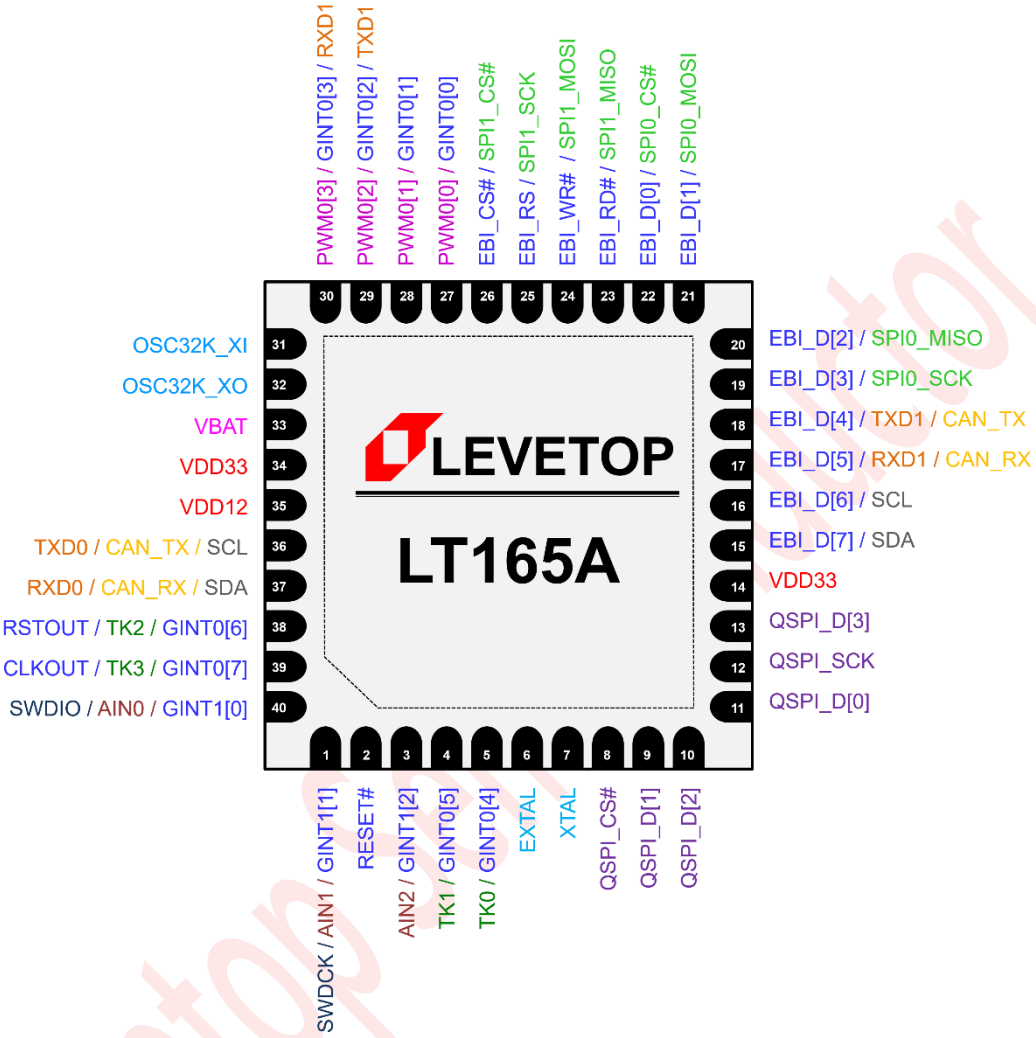

Figure 2-1: LT165A (QFN-40) Pin Assignment

2.2. Signal Properties Summary

Table 2-1: Signal Properties

Name	Alternate 0	Alternate 1	GPIO	Default State	Default Dir *1	Pullup *2	IO Type *3
SCI (2)							
TXD0	SCL	CAN_TX	GIOP29	HiZ	--	--	I/O
RXD0	SDA	CAN_RX	GPIO30	HiZ	--	--	I/O
QSPI (6)							
QSPI_CS#	--	--	GPIO19	HiZ	--	--	I/O
QSPI_D[0]	--	--	GPIO20	HiZ	--	--	I/O
QSPI_D[1]	--	--	GPIO21	HiZ	--	--	I/O
QSPI_D[2]	--	--	GPIO22	HiZ	--	--	I/O
QSPI_D[3]	--	--	GPIO23	HiZ	--	--	I/O
QSPI_SCK	--	--	GPIO24	HiZ	--	--	I/O
PWM0 (4)							
PWM0[0]	GINT0[0]	COMP0_OUT	GPIO0	HiZ	--	--	I/O
PWM0[1]	GINT0[1]	--	GPIO1	HiZ	--	--	I/O
PWM0[2]	GINT0[2]	TXD1	GPIO2	HiZ	--	--	I/O
PWM0[3]	GINT0[3]	RXD1	GPIO3	HiZ	--	--	I/O
ADC (1)							
AIN2	GINT1[2]	--	GPIO18	HiZ	--	--	I/O
Touch (2)							
TK0	GINT0[4]	--	GPIO4	HiZ	--	--	I/O
TK1	GINT0[5]	--	GPIO5	HiZ	--	--	I/O
Programming Port (2)							
SWDIO	GINT1[0]	AIN0	GPIO16	I	I	PullUp	I/O
SWDCK	GINT1[1]	AIN1	GPIO17	I	I	PullUp	I/O
CLOCK (5)							
EXTAL	--	--	--	HiZ/I	--/I	--	I
XTAL	--	--	--	HiZ/O	--/O	--	O
OSC32K_XI	--	--	--	I	I	-	I
OSC32K_XO	--	--	--	O	O	--	O
CLKOUT	GINT0[7]	TK3	GPIO7	O	O	--	I/O
RESET (2)							
RESET#	--	--	--	I	I	PullUp	I
RSTOUT	GINT0[6]	TK2	GPIO6	O	O	--	I/O
EBI (12)							

Name	Alternate 0	Alternate 1	GPIO	Default State	Default Dir *1	Pullup *2	IO Type *3
EBI_CS#	SPI1_CS#	--	GPIO25	HiZ	--	--	I/O
EBI_RS	SPI1_SCK	--	GPIO28	HiZ	--	--	I/O
EBI_RD#	SPI1_MISO	--	GPIO27	HiZ	--	--	I/O
EBI_WR#	SPI1_MOSI	--	GPIO26	HiZ	--	--	I/O
EBI_D[0]	SPI0_CS#	--	GPIO8	HiZ	--	--	I/O
EBI_D[1]	SPI0_MOSI	--	GPIO9	HiZ	--	--	I/O
EBI_D[2]	SPI0_MISO	--	GPIO10	HiZ	--	--	I/O
EBI_D[3]	SPI0_SCK	--	GPIO11	HiZ	--	--	I/O
EBI_D[4]	TXD1	CAN_TX	GPIO12	HiZ	--	--	I/O
EBI_D[5]	RXD1	CAN_RX	GPIO13	HiZ	--	--	I/O
EBI_D[6]	SCL	--	GPIO14	HiZ	--	--	I/O
EBI_D[7]	SDA	--	GPIO15	HiZ	--	--	I/O
Power Supply (5)							
VDD33	--	--	--	P	--	--	--
VDD12	--	--	--	P	--	--	--
AVDD	--	--	--	P	--	--	--
VBAT	--	--	--	P	--	--	--
VSS	--	--	--	G	--	--	--

NOTE:

1. 'Default Dir' refers to the direction after resetting. 'I' represents input, 'O' represents output, 'O (H)' represents output high, 'O (L)' represents output low, 'Hiz' represents both input and output disabled, and pull-up/pull-down is also disabled.

2. When the signal is set to output, all pull-up and pull-down are disconnected.

3. 'IO TYPE' refers to the pin design: 'I' represents a pin that only has input function; 'O' represents only the output function pin; 'I/O' represents a pin that has both input and output functions.

2.3. Signal Description

This chapter provides a brief explanation of pin signals. For more detailed information, please refer to the specific module section.

Tabel 2-2: Signal Description

Pin Name	Pin Number	Pin Description
Serial Communications Interface – 0, SCI0		
RXD0	37	**SCI (Uart) 0 Receive Data** This signal is used for SCI0 receiver data input. This signal can be configured as the SCI0 receiver data input, or be configured as SDA, CAN_RX or GPIO30. Please refer to Table 2-1 for information on share-used signals.
TXD0	36	**SCI (Uart) 0 Transmit Data** This signal is used for SCI0 transmitter data output. This signal can be configured as the SCI0 transmitter data output, or be configured as SCL, CAN_RX or GPIO29.
Serial Communications Interface – 1, SCI1		
RXD1	17 / 30	**SCI (Uart) 1 Receive Data** This signal is used for SCI1 receiver data input This signal has two multiplexing sources, one of which is share-used with EBI-D [5], CAN-RX, or GPO13 signals. The other is to share-used with PWM0[3], GINT0 [3], or GPIO3 signals.
TXD1	18 / 29	**SCI (Uart) 1 Transmit Data** This signal is used for SCI1 transmitter data output. This signal has two multiplexing sources, one of which is share-used with EBI-D [4], CAN_TX, or GPO12 signals. The other is share-used with PWM0[2], GINT0 [2], or GPIO2 signals.
CAN Bus		
CAN_RX	17 / 37	**Can Bus Receive Data** This signal comes from the receiving pin of the CANBus transceiver. The explicit state is represented by the logic level '0'. The implicit state is represented by the logic level "1". This signal has two multiplexing sources. When not configured for CANBUS operation, one is share-used with EBI-D [5], RXD1, or GPOI13 signals, and the other is share-used with RXD0, SDA, or GPIO30 signals.
CAN_TX	18 / 36	**Can Bus Transmit Data** This signal is the sending pin of the CANBus transceiver. The explicit state is represented by the logic level '0'. The implicit state is represented by the logic level "1". This signal has two multiplexing sources. When not configured for CANBUS operation, one is share-used with EBI-D [4], TXD1, or GPIO12 signals, and the other is share-used with TXD0, SCL, or GPIO29 signals.
External Bus Interface, EBI The external bus interface is responsible for controlling the information transmission between the internal bus and the external MCU type TFT LCD panel. Only LT165A supports 8bit EBI interface.		

Pin Name	Pin Number	Pin Description
EBI_CS#	26	**EBI Chip Selection (8080 I/F Panel Chip Selection)** LT165A provides an External Bus Interface (EBI) to drive the TFT LCD display panel of the 8bit 8080 interface, and this signal is the chip selection of the external bus interface. This signal is share-used with SPI1_CS# or GPIO25.
EBI_RS	25	**EBI Register Selection Signal** This signal is connected to the RS or A0 of the 8Bit LCD panel. This signal is share-used with SPI1_SCK or GPIO28.
EBI_RD#	23	**EBI Data Reading Control Signal** This signal is the control signal for LT165 to read data from the external 8Bit LCD panel. This signal is share-used with SPI1_MISO or GPIO27.
EBI_WR#	24	**EBI Data Writing Control Signal** This signal is the control signal for LT165 to write data to the external 8Bit LCD panel. This signal is share-used with SPI1_MOSI or GPIO26.
EBI_D[0]	22	**EBI Data Signal 0** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with SPI0_CS# or GPIO8.
EBI_D[1]	21	**EBI Data Signal 1** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with SPI0_MOSI or GPIO9.
EBI_D[2]	20	**EBI Data Signal 2** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with SPI0_MISO or GPIO10 signal.
EBI_D[3]	19	**EBI Data Signal 3** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with SPI0_SCK or GPIO11.
EBI_D[4]	18	**EBI Data Signal 4** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with TXD1, CAN_TX or GPIO12.
EBI_D[5]	17	**EBI Data Signal 5** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with RXD1, CAN_RX or GPIO13.
EBI_D[6]	16	**EBI Data Signal 6** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with SCL or GPIO14.

Pin Name	Pin Number	Pin Description
EBI_D[7]	15	**EBI Data Signal 7** This signal is the data Bit0 transmission signal from LT165 to the external 8Bit LCD panel. This signal is share-used with SDA or GPIO15.
I2C		
SCL	16 / 36	**I2C Clock Signal** This signal is used for I2C clock line signal. This signal has two multiplexing sources. When not configured for I2C operation, one is share-used with EBI-D [6] or GPIO14 signals, and the other is share-used with TXD0, CAN_TX, or GPIO29.
SDA	15 / 37	**I2C Data** This signal is used for I2C data line signals. This signal has two multiplexing sources. When not configured for I2C operation, one is share-used with EBI-D [7] or GPIO15 signals, and the other is share-used with RXD0, CAN-RX, or GPIO30 signals.
QSPI		
QSPI_D[3:0]	13, 10, 9 11	**QSPI Data Input/Output** These signals are the data outputs or inputs of QSPI in master mode.
QSPI_CS#	8	**QSPI Chip Select Signal** This signal is the chip select output of QSPI in master mode, and active low.
QSPI_SCK	12	**QSPI Clock Signal** This signal is the clock output of QSPI in master mode.
SPI		
SPI0_MOSI	21	**SPI #0 Data Output** This signal is the data output of the first group SPI. This signal is share-used with EBI_D[1] or GPIO9.
SPI0_MISO	20	**SPI #0 Data Input** This signal is the data input of the first group SPI. This signal is share-used with EBI_D[2] or GPIO10.
SPI0_CS#	22	This signal is the chip select output of the first group SPI. This signal is share-used with EBI_D[0] or GPIO8.
SPI0_SCK	19	**SPI #0 Serial Clock Signal** This signal is the clock output of the first group SPI. This signal is share-used with EBI_D[3] or GPIO11.
SPI1_MOSI	24	**SPI #1 Data Output** This signal is the data output of the second group SPI. This signal is share-used with EBI_WR# or GPIO26.
SPI1_MISO	23	**SPI #1 Data Input** This signal is the data input of the second group SPI. This signal is share-used with EBI_RD# or GPIO27.

Pin Name	Pin Number	Pin Description
SPI1_CS#	26	**SPI #1 Chip Select Signal** This signal is the chip select output of the second group SPI. This signal is share-used with EBI_CS# or GPIO25.
SPI1_SCK	25	**SPI #1 Serial Clock Signal** This signal is the clock output of the second group SPI. This signal is share-used with EBI_RS or GPIO28.
Touch Key		
TK0	5	**Touch Key 0** Input This signal is share-used with GINT0[4] or GPIO4.
TK1	4	**Touch Key 1** Input This signal is share-used with GINT0[5] or GPIO5.
TK2	38	**Touch Key 2** Input This signal is share-used with RSTOUT, GINT0[6] or GPIO6.
TK3	39	**Touch Key 2** Input This signal is share-used with CLKOUT, GINT0[7] or GPIO7. ◦
EPORT 0		
GINT0[0]	27	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with PWM0[0], COMP0_OUT or GPIO0.
GINT0[1]	28	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with PWM0[1] or GPIO1.
GINT0[2]	29	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with PWM0[2], TXD1 or GPIO2.
GINT0[3]	30	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with PWM0[3], RXD1 or GPIO3.
GINT0[4]	5	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with TK0 or GPIO4.
GINT0[5]	4	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with TK1 or GPIO5.

Pin Name	Pin Number	Pin Description
GINT0[6]	38	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with RSTOUT, TK2 or GPIO6.
GINT0[7]	39	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with CLKOUT, TK3 or GPIO7.
EPORT 1		
GINT1[0]	40	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with SWDIO, AIN0 or GPIO16.
GINT1[1]	1	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with SWDCK, AIN1 or GPIO17.
GINT1[2]	3	**Interrupt Input / GPIO** These bidirectional signals can be used as external interrupt sources or GPIO. This signal is share-used with AIN2 or GPIO18.
PWM 0		
PWM0[3:0]	30, 29, 28, 27	**PWM Output** These output signals can be used as PWM0 outputs, GINT0[3:0] or GPIO[3:0].
ADC		
AIN2	3	**Analog Input Signal** This analog signal is used as an ADC analog input channel. When not configured as an analog input, this signal can also be used for GINT1[2] or GPIO18.
AIN1	1	**Analog Input Signal** This analog signal is used as an ADC analog input channel. When not configured as an analog input, this signal can also be used for SWDCK, GINT1[1] or GPIO17.
AIN0	40	**Analog Input Signal** This analog signal is used as an ADC analog input channel. When not configured as an analog input, this signal can also be used for SWDIO, GINT1[0] or GPIO16.
Programming Signals		

Pin Name	Pin Number	Pin Description
SWDCK	1	**MCU Code Programming Clock** This input signal is the clock signal used for programming internal flash memory. When not configured as an analog input, this signal can also be used for GINT1[1], AIN1 or GPIO17.
SWDIO	40	**MCU Code Programming Data** This signal is used as a data signal for programming internal flash memory. When not configured as SWDIO, this signal can also be used for GINT1[0], AIN0 or GPIO16.
Clock		
EXTAL	6	**System Oscillator Input** The signal is the input of 24MHz Oscillator Pad.
XTAL	7	**System Oscillator Output** The signal is the output 24MHz Oscillator pad.
OSC32K_XI	31	**32.768KHz Oscillator Input** The signal is the input of 32.768KHz Oscillator pad.
OSC32K_XO	32	**32.768KHz Oscillator Output** The signal is the output 32.768KHz Oscillator pad.
CLKOUT	39	**Clock Out** This output signal reflects the internal system clock. When not configured as Clock output, this signal can also be configured as GINT0[7], TK3 or GPIO7.
Reset		
RESET#	2	**Reset Input Signal** When RESET#=0, a reset action will be performed on the internal MCU. Except for a few registers that can only be reset by POR, most registers controlled by MCU will return to their default values.
RSTOUT	38	**Reset Output Signal** This output signal indicates that the internal reset controller is resetting the chip. 0=The chip is in a reset state 1=chip not reset state When not configured as a reset output, this signal can also be share-used for GINT0 [6], TK2, or GPIO6.
Power and Grounding Signals These signals provide system power and grounding for the chip. It is necessary to ensure that the chip can obtain sufficient current capability. All power signals must have sufficient bypass capacitance to suppress high-frequency noise.		
VDD33	14, 34	**3.3V Power Input** This signal supplies 3.3V positive power to the I/O pads and LDO.

Pin Name	Pin Number	Pin Description
VDD12	35	**1.2V LDO Output** This 1.2V LDO output signal is used to supply the power of the core logic. One 1uF and one 0.1uF ceramic bypass capacitors are required to externally connect between the pad and VSS.
AVDD	--	**3.3V Analog Power Input** This signal supplies 3.3V positive power to ADC module.
VBAT	33	**RTC Power** This signal supplies battery power to RTC module.
VSS	41(*)	This signal supplies 3.3V negative supply (ground) to the I/O pads and LDO.

NOTE: *This is a thermal pad zone that must be connected to VSS or GND. When making PCB layout, special attention should be paid to the solder surface design of the pads. Please refer to Section 7.2 for details.*

2.4. LT165A Resource

Table 2-3: LT165A Resource

Functions		LT165A
Items	**Description**	
TFT LCD Panel	8bit 8080 I/F	√
	SPI I/F	√
MCU	MCU Core	32bits RISC
	MCU Clock	150MHz
	SRAM	32KB
Interface	SCI (Uart)	√ (x2)
	SPI	√ (x2)
	QSPI	√ (x1)
	PWM O/P	√ (x4)
	Can Bus	√ (x1)
	ADC I/P	√ (x3)
	Touch Key	√ (x4)
	CTP I2C I/F	√
	GPIO Port	√ (x11)
	RTC	√
Application	UI_Editor-II	√
	UI_Emulator-II	√
	Uart Port Upgrade	√
	Support 2nd Develop	√
Power & Package	Power	3.3V
	Package	QFN-40

3. Hardware Interface

3.1. Host Communication Interface

The communication between LT165 and the Host MCU is through SCI (UART) interface. The UART interfaces TX and RX on both sides must be cross docked, as shown in the following figure. If the connection distance is long, an RS232 driver chip needs to be added to avoid signal attenuation affecting communication. The software settings and communication protocol for serial Uart can refer to the application note (UI-Editor-II_CH_Vxx.pdf) of Levetop Semiconductor.

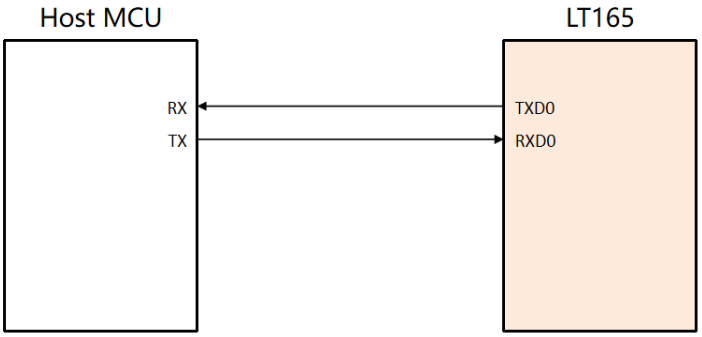

Figure 3-1: UART Connection Between LT165 and Host MCU

3.2. TFT LCD Panel Interface

LT165A provides an External Bus Interface (EBI) for driving a TFT LCD panel with a parallel 8bit 8080 interface. The schematic diagram is shown in Figure 3-2 below:

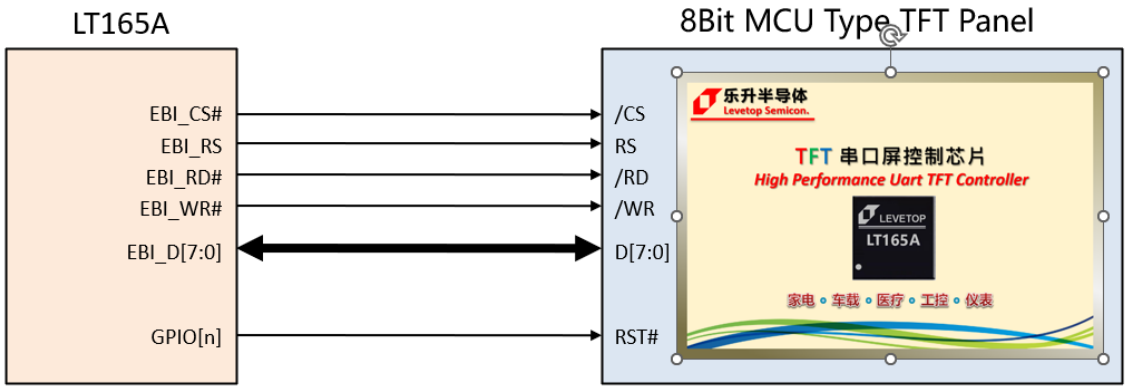

Figure 3-2: LT165A Connect to 8bits 8080 I/F of TFT LCD Panel

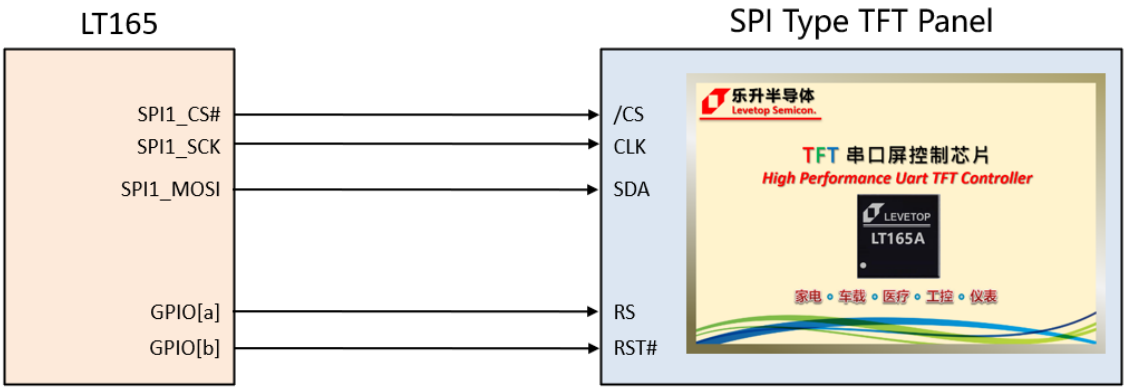

Figure 3-3: LT165 Connect to SPI I/F of TFT LCD Panel

3.3. QSPI Interface

LT165 has a set of QSPI interfaces for connecting to external QSPI Flash. This external Flash is used to store program code, display images, animations, text, and other information. When LT165 receives a serial command sent by the main control through the Uart interface, it will extract images or other display related information from QSPI Flash according to the command and transmit it to the LCD panel. The reference schematic is shown in the following figure.

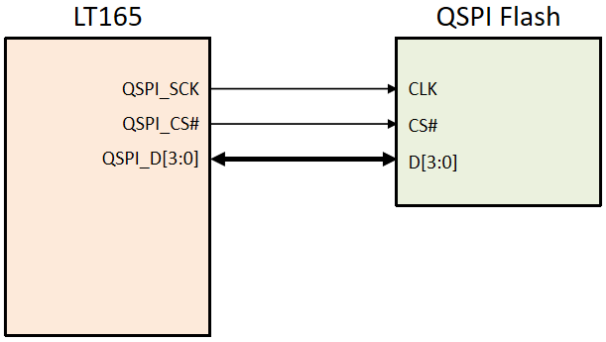

Figure 3-4: LT165 Connect to QSPI Flash

3.4. LCD Touch Panel Interface

LT165 has an ADC module and I2C interface that can be used to interface directly to resistive or capacitive touch panel. Upon receiving the touch information, LT165 will process it and transmit it to the Host MCU. The reference schematic is as followings:

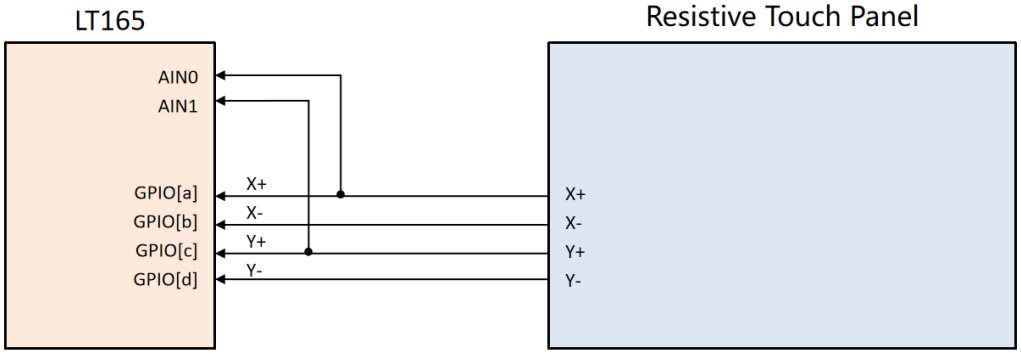

Figure 3-5: LT165 Connect to Resistive Touch Panel

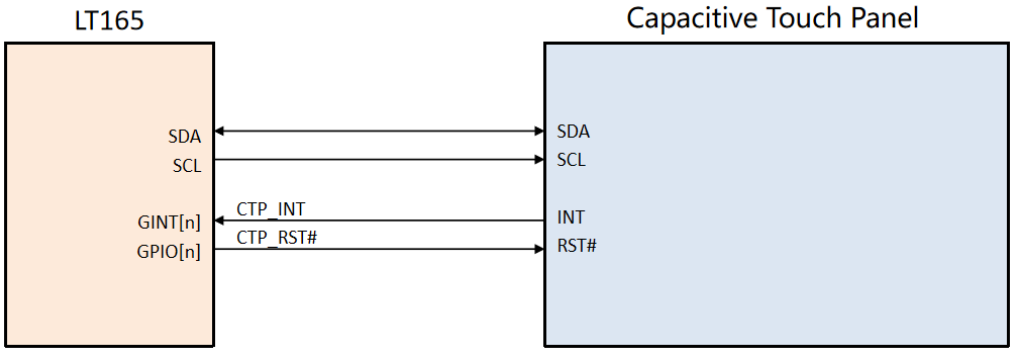

Figure 3-6: LT165 Connect to Capacitive Touch Panel

3.5. Clock Interface

LT165A requires an external 12MHz crystal oscillator as the internal system clock source. The reference schematic is as follows:

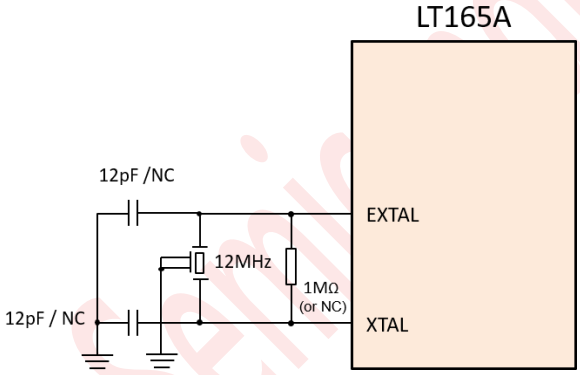

Figure 3-7: External 12MHz Clock Circuit

3.6. Can Bus Interface

LT165 supports the Can Bus protocol and provides a set of Can Bus interfaces When in use, an additional Can Bus driver chip is required to communicate with the external environment. Please refer to the schematic diagram below:

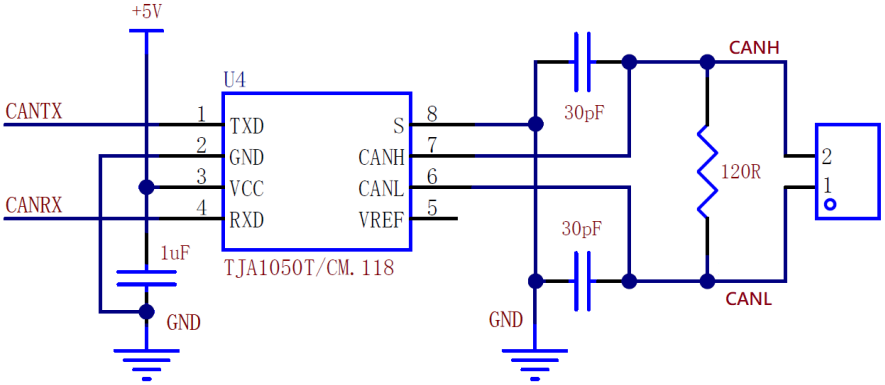

Figure 3-8: Canbus Circuit Example

3.7. LCD Backlight Control Circuit

LT165 uses PWM1[3] to provide a backlight control signal - "BL_PWM" that can be used to control TFT LCD panel backlight. The reference schematics are as followings:

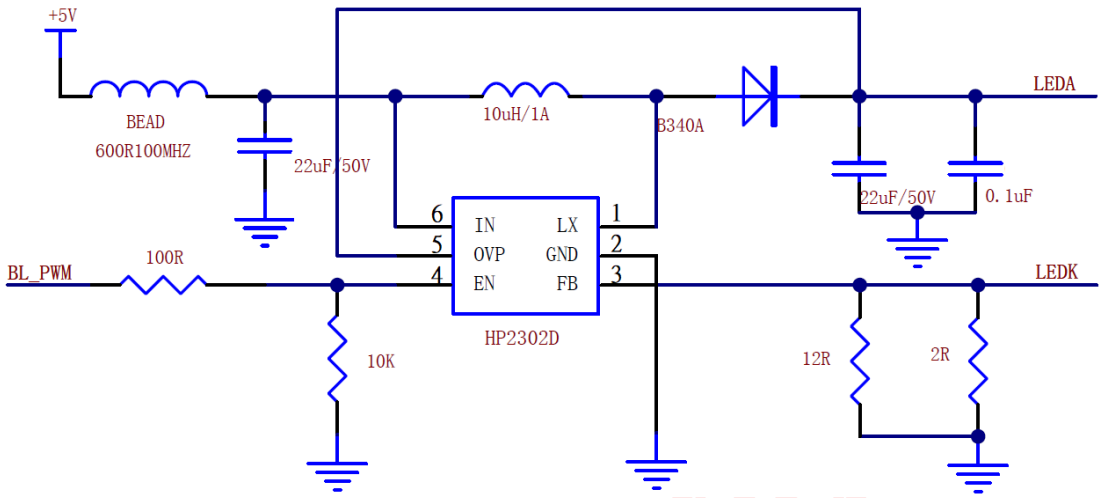

Figure 3-9: TFT LCD Backlight Circuit Example 1

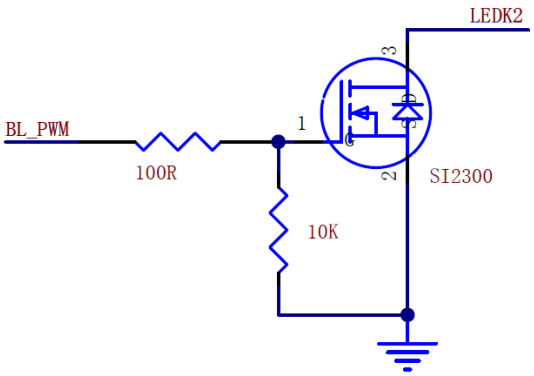

Figure 3-10: TFT LCD Backlight Circuit Example 2

3.8. Real Time Clock (RTC)

The LT165 has an RTC (Real Time Clock) clock module inside If using this RTC clock, a 32.768KHz crystal oscillator circuit is required RTC is independently powered, and if RTC continues to operate even when the external power is turned off, an external battery power can be added The reference schematic diagram is as follows:

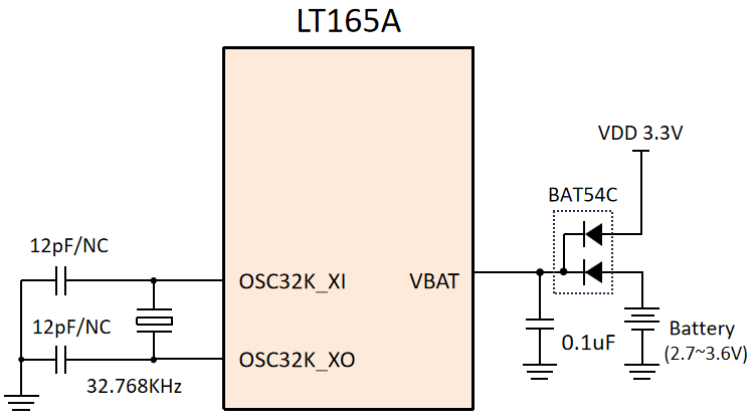

Figure 3-11: RTC Application Circuit

3.9. Reset Interface

There are two hardware reset sources for LT165, both of which are synchronized by the internal clock:

– Power on Reset

– External Reset Pin (RESET#)

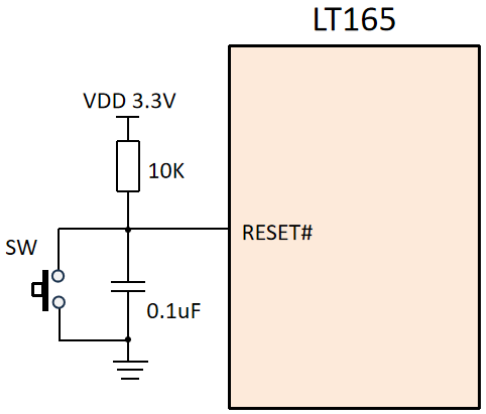

Figure 3-12: External Reset Circuit

4. System Memory Map

4.1. Introduction

The built-in memory, registers, and external memory of LT165 include:

- Up to 128M Bytes of External QSPI Flash
- 8K Bytes Internal Boot ROM
- 32K Bytes Internal Static SRAM
- Internal Memory Mapped Registers

4.2. Memory Address Map

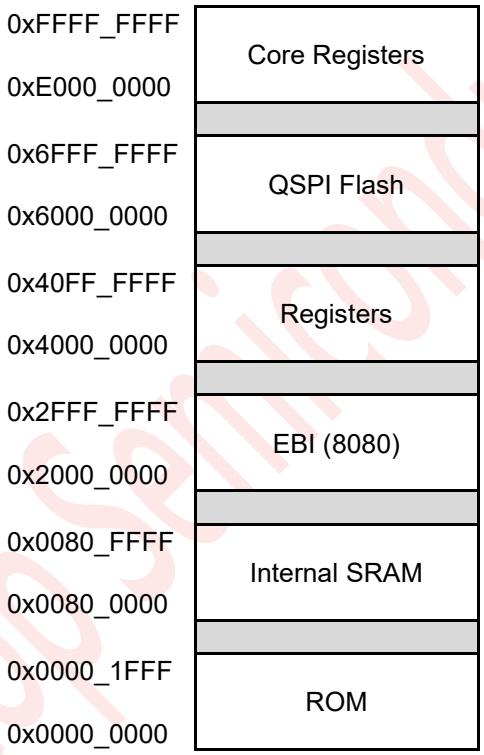

Figure 4-1: Memory Address Map

Table 4-1: The Hardware Module and Register Address Location Map

Address	Maximum Size	Hardware Module
0x4000_0000	64Kbyte	Direct Memory Access Controller (DMAC)
0x4001_0000	64Kbyte	System Integration Module (SIM)
0x4002_0000	64Kbyte	Reset Control Module (RCM)
0x4003_0000	64Kbyte	Clock Control Module (CLKM)
0x4004_0000	64Kbyte	Programmable Interrupt Timer 0 (PIT0)
0x4005_0000	64Kbyte	Programmable Interrupt Timer 1 (PIT1)
0x4006_0000	64Kbyte	Reserved

Address	Maximum Size	Hardware Module
0x4007_0000	64Kbyte	Reserved
0x4008_0000	64Kbyte	Serial Communication Interface 1 (SCI1)
0x4009_0000	64Kbyte	Serial Communication Interface 0 (SCI0)
0x400A_0000	64Kbyte	Analog Comparator 0 (COMP0)
0x400B_0000	64Kbyte	Reserved
0x400C_0000	64Kbyte	Reserved
0x400D_0000	64Kbyte	Pulse Width Modulator 0 (PWM0)
0x400E_0000	64Kbyte	Reserved
0x400F_0000	64Kbyte	Edge Port Module 0 (EPORT0)
0x4010_0000	64Kbyte	Edge Port Module 1 (EPORT1)
0x4011_0000	64Kbyte	Analog-to-Digital Convertor (ADC)
0x4012_0000	64Kbyte	Option Byte (OPB)
0x4013_0000	64Kbyte	WatchDog Timer (WDT)
0x4014_0000	64Kbyte	Real Time Controller (RTC)
0x4015_0000	64Kbyte	Inter-Integrated Circuit (I2C)
0x4016_0000	64Kbyte	Touch Controller
0x4017_0000	64Kbyte	Crossbar Switch (XBAR)
0x4018_0000	64Kbyte	External Bus Interface (EBI)
0x4019_0000	64Kbyte	CACHE Module (CACHEM)
0x401A_0000	64Kbyte	Reserved
0x401B_0000	64Kbyte	Reserved
0x401C_0000	64Kbyte	CANBus Controller (CANBC)
0x401D_0000	64Kbyte	Reserved
0x401E_0000	64Kbyte	Serial Peripheral Interface Module - SPI0
0x401F_0000	64Kbyte	Serial Peripheral Interface Module - SPI1
0x6000_0000	64Kbyte	Synchronous Serial Interface 0 (SSI0) - QSPI0
0xE000_0000	4Kbyte	Embedded Interrupt Controller (EIC)
0xE000_1000	4Kbyte	Embedded Programmable Timer (EPT)

Note: For detailed register configuration, please refer to the complete specification sheet.

5. Electrical Characteristic

This chapter provides the electrical characteristic parameters and limits for LT165.

5.1. Absolute Maximum Ratings

Table 5-1: Absolute Maximum Rating

Symbol	Item	Range	Unit
V_{DD33}	Power Supply	-0.5 ~ 4.6	V
V_{IN}	Input Voltage Range	-0.5 ～ VDD33+0.5	V
V_{OUT}	Output Voltage Range	-0.5 ～ VDD33+0.5	V
P_D	Power Dissipation	≦300	mW
T_{OPR}	Operation Temperature	-40 ~ 105	℃
T_{JT}	Operation Junction Temperature	-40 ~ 125	℃
T_{ST}	Storage Temperature	-55 ~ 150	℃
T_{SOL}	Soldering Temperature	260	℃

NOTE: If the loading to the chip exceeds the absolute maximum rating listed in **Table 5-1**, it may result in permanent damage to the chip. Although the chip contains circuitry to resist damage from high quiescent voltages, do not apply more voltages on the chip than the values rated in the table. These values are only ratings and do not mean that the chip functions properly under these conditions.

5.2. DC Electrical Specification

Table 5-2: IO Static Characteristic (3.3V)

Item	Symbol	Min	Typical	Max	Unit
IO Supply Power	VDD33	VOP_L(*1)	3.3	3.63	V
Input High Voltage	V_{IH}	2.0	-	VDD33+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Output High Voltage	V_{OH}	VOP_L*0.8	-	VDD33	V
Output Low Voltage	V_{OL}	0	-	0.4	V
Input Leakage Current	I_{IN}	-	-	1	uA
Pull-Up Resistor	RPU	33	41	62	KΩ
Pull-Down Resistor	RPD	33	42	68	KΩ

Note: Refer to following Table 5-4.

Table 5-3: Power Characteristic

Item	Symbol	Min	Typical	Max	Unit
Chip Power	VDD33	VOP_L	3.3	3.63	V
ADC Power I/P	AVDD	VOP_L	3.3	3.63	V
Chip Core Power (LDO O/P)	VDD12	1.1	1.2	1.3	V
RTC Power	VBAT	1.7	3.3	3.6	V

Table 5-4: PVDC Setting Table vs. VOP_L

PVDC	Detect Voltage	VOP_L
2'b00	2.16V	2.31V
2'b01	2.32V	2.47V
2'b10	2.48V	2.63V
2'b11	2.64V	2.79V

Note:

1. PVDC is Programmable Voltage Detector Configuration Registe, please refert to section 14.1.1 of complete data sheet for detail.
2. Because the code configuration of LT165A is within the external SPI Flash, the minimum operating voltage of SPI Flash needs to be lower than the set voltage of VOP_L.

5.3. Electrostatic Discharge (ESD) Protection

Table 5-5: Electrostatic Discharge Protection Characteristic

ESD Test	Symbol	Max	Unit	Reference Standard
Human Body Model	HBM	±4,000	V	ANSI/ESDA/JEDEC JS-001-2017
Machine Model	MM	200	V	JEDEC JESD22-A115C-2010
Charged Device Model	CDM	±1000	V	ANSI/ESDA/JEDEC JS-002-2022
Latch Up	LU	±200	mA	JEDEC JESD78F.01-2022, @25℃

Note: When performing manual soldering, it is recommended that personnel and equipment should be treated with anti-static. For example, appropriate temperature and humidity environment, grounding of welding equipment, anti-static workbench, and welding personnel wearing anti-static wrist straps, etc.

5.4. VDD Power Up Timing

When using the LT165x, it is important to pay attention to the power up requirements of VDD. The VDD33 must maintain a waiting time of at least 400ms at the low voltage (V_L) at the time of power-up (T_{WAIT}). At the same time, the rise time (T_R) of VDD33 from V_L to normal operating voltage should not be too long. The normal operating voltage range must be reached within 500ms. Otherwise, the MCU inside the LT165 will not boot properly.

Table 5-6: VDD Power Up Characteristic

Item	Symbol	Description	Min.	Nom.	Max.	Unit
Rise Time	T_R	The rise time of input voltage from V_L to the normal operating voltage	-	-	500	ms
Wait Time	T_{WAIT}	The retention time of the V_L before Power On	400	-	-	ms
VDD Input Voltage	V_L	at T=T_1 on pin VDD33 (The input voltage before Power Up)	-	-	200	mV
VDD Input Voltage	V_H	Normal Operation Voltage	2.97	3.3	3.63	V

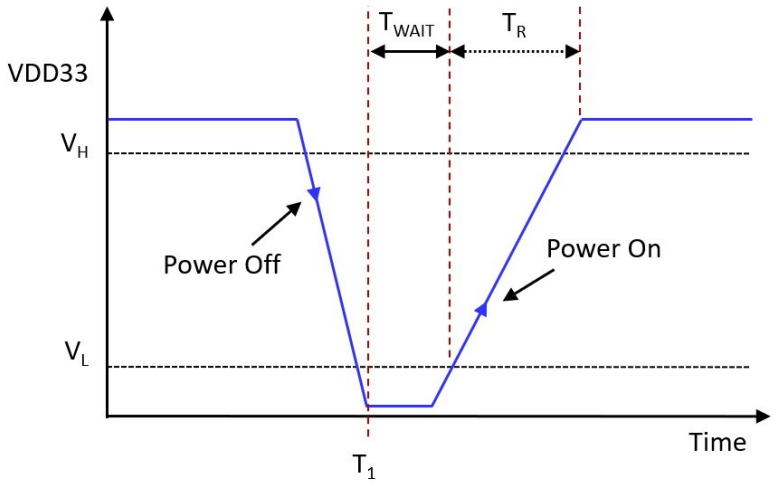

Figure 5-1: VDD Power up Timing Requirement

6. Application Circuit

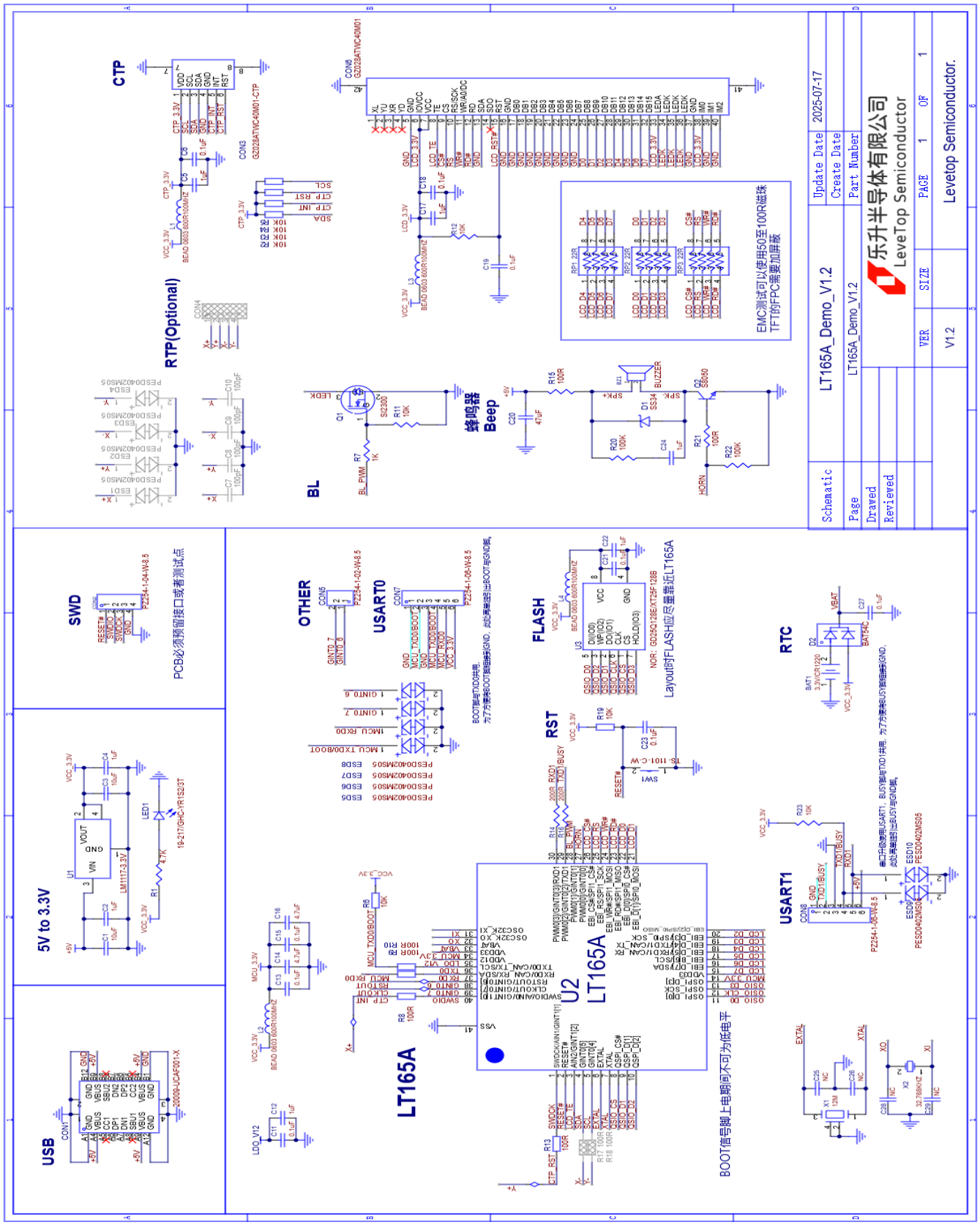

Figure 6-1: AP Circuit of LT165A for 8bit 8080 Interface TFT LCD Panel

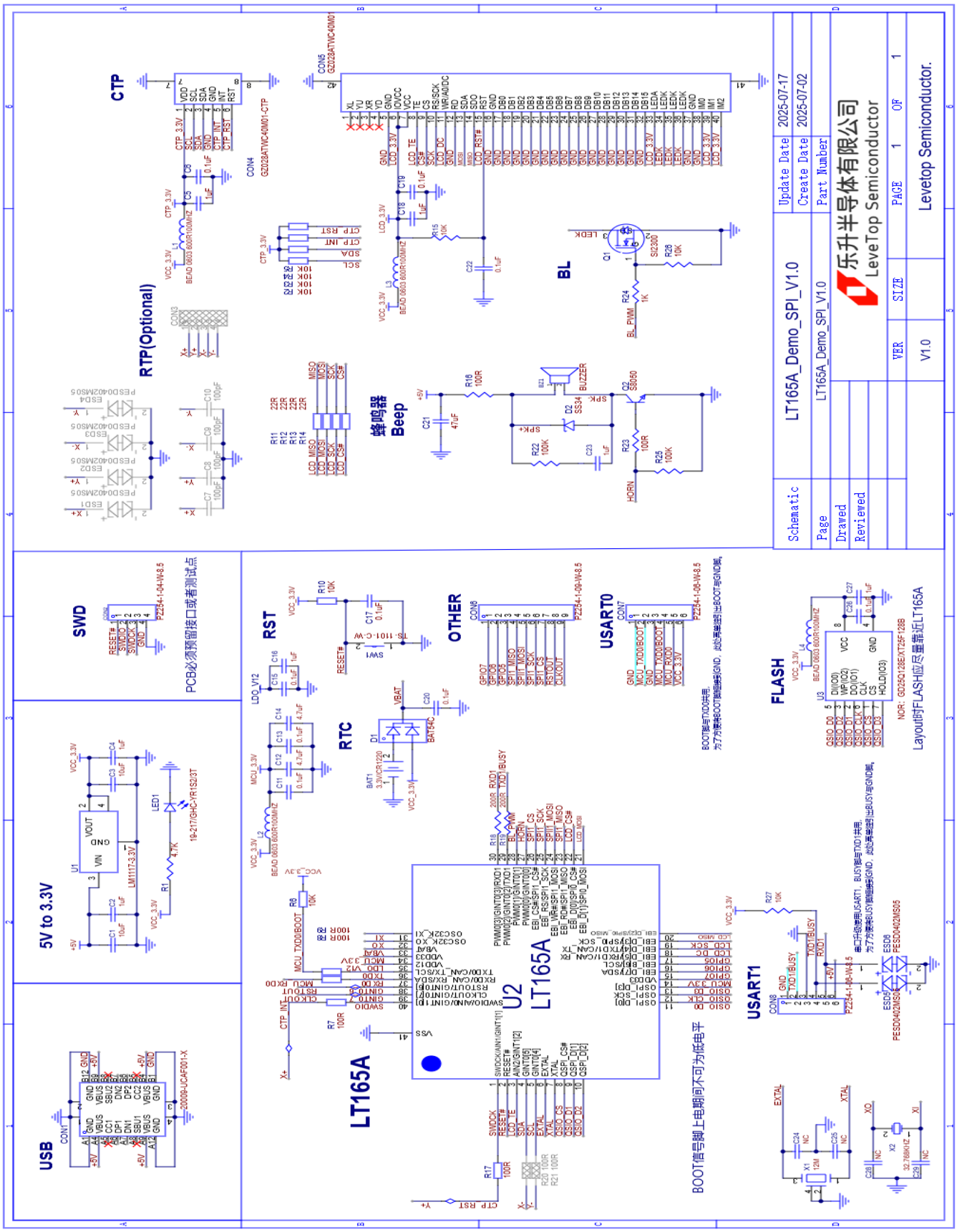

Figure 6-2: AP Circuit of LT165A for SPI Interface TFT LCD Panel

7. Package

7.1. LT165A (QFN-40pin)

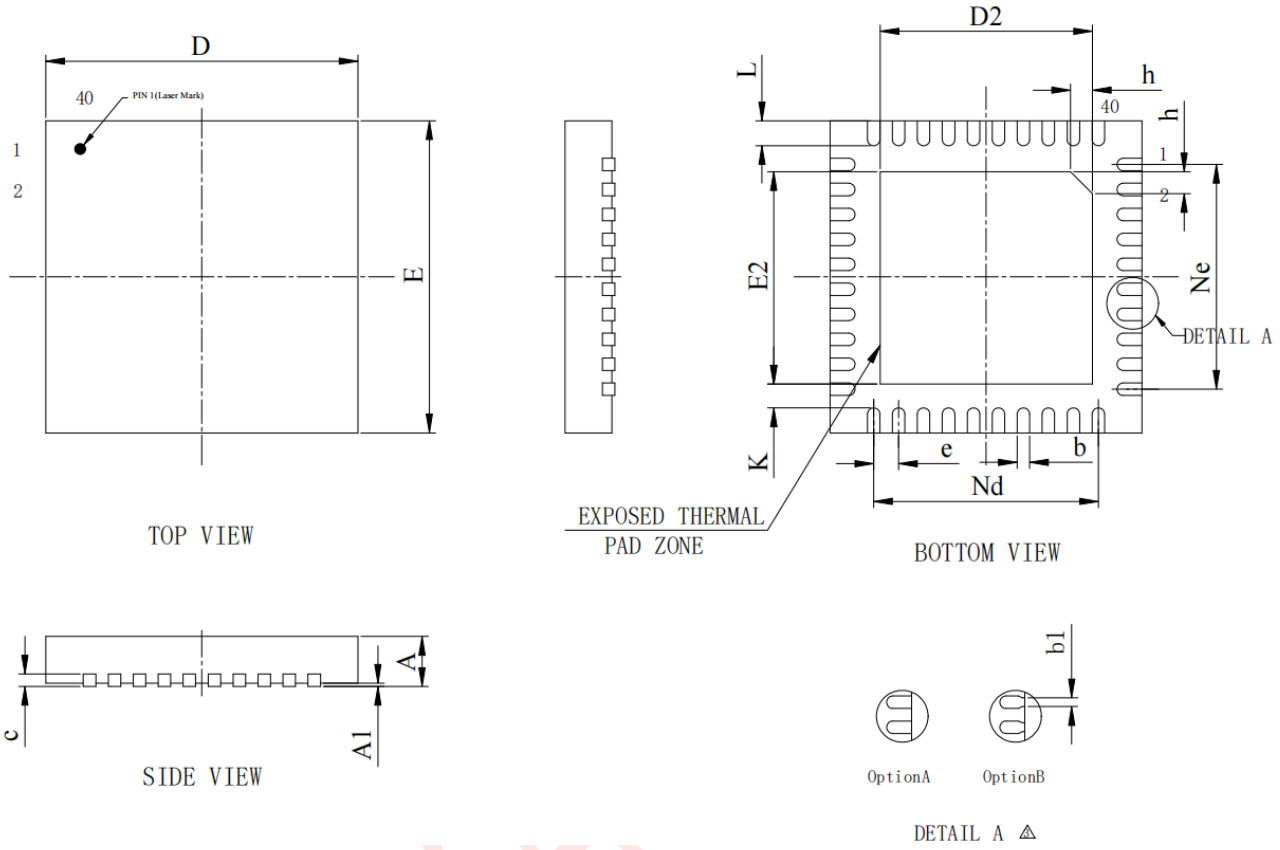

Figure 7-1: LT165A Package Overview

Note: When layout PCB, LT165A Thermal Pad Zone must be connected to ground. Please refer to Section 7.3 for PCB routing of ground thermal pad.

Table 7-1: LT165A Package Parameter

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	0.70	0.75	0.80	Nd	3.6BSC		
A1	--	0.02	0.05	E	4.90	5.00	5.10
b	0.15	0.20	0.25	E2	3.30	3.40	3.50
b1	0.14REF			Ne	3.60BSC		
c	0.18	0.25	0.30	L	0.35	0.40	0.45
D	4.90	5.00	5.10	K	0.20	--	--
D2	3.30	3.40	3.50	h	0.30	0.35	0.40
e	0.40BSC						

7.2. PCB Design for Ground Pad

The LT165A is available in a QFN package with a ground (GND) thermal pad on the back of the chip. In order to achieve better heat dissipation and reduce the risk of soldering, it is recommended to divide the copper surface of the PCB on the bottom pad of LT165A into four small solder surfaces (square or round) when laying out the PCB. And the spacing between each soldering surface is set at ~0.8mm, so as to avoid incomplete soldering caused by the PCB using a complete soldering surface that is the same or even larger than the size of the LT165A pad, or the chip deformation and poor contact caused by the pulling of the PCB and the chip pad after soldering cooling.

The correct PCB pad layout is shown in the following examples, the light yellow area in the middle is the ground pad at the bottom of the LT165A, and the gray area is the small PCB ground pad (solder surface). Each pad has 1~2 vias grounded.

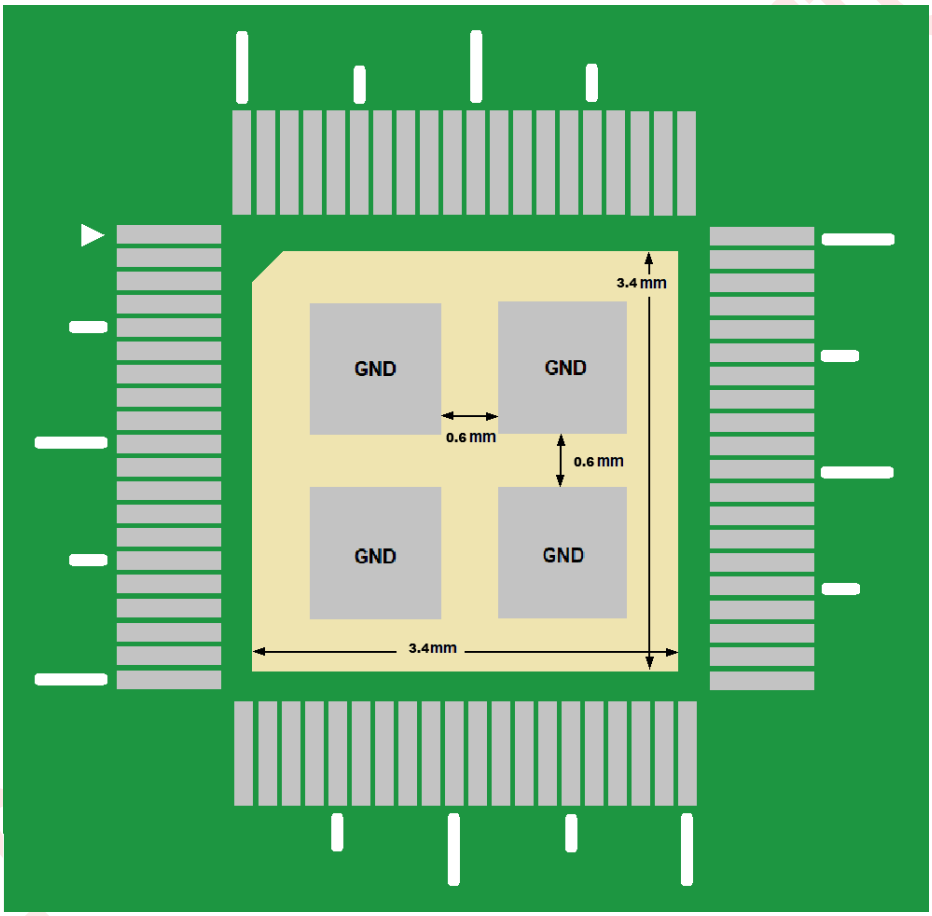

Figure 7-2: PCB Design Recommendation for the LT165A Bottom Ground Pad