乐升半导体
LEVETOP

LT32U02
LT32A02

High Performance 32bit Micro Controller

Introduction

The LT32x02 incorporates the High-performance C0 32-bit RISC core operating at a 72MHz maximum frequency with high-speed embedded Flash memories (Flash up to 64Kbytes which contains an 1kbytes two-way set associative read Cache and SRAM up to 8Kbytes), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces, including two Master SPI, one I2C, one UART. The LT32U02 also provide one USB2.0 Fast Speed controller. Both of LT3202 support up to four General-purpose 16-bit timers, one embedded programmable 24-bit timers, eight advanced-control PWM timers and two asynchronous Watch Dog Timers. It also provides Analog modules including one 1MSPS ADC with 8-channels and two Comparators.

The LT32U02 is QFN-48pin package, LT32A02 is QFN-32pin package. The operation temperature range is -40°C to 85°C and the operating voltage is 2.0/2.8~5.5V.

Package Types

LT32U02

QFNWB6X6-48L

LT32A02

QFNWB5X5-32L

Pin Assignment

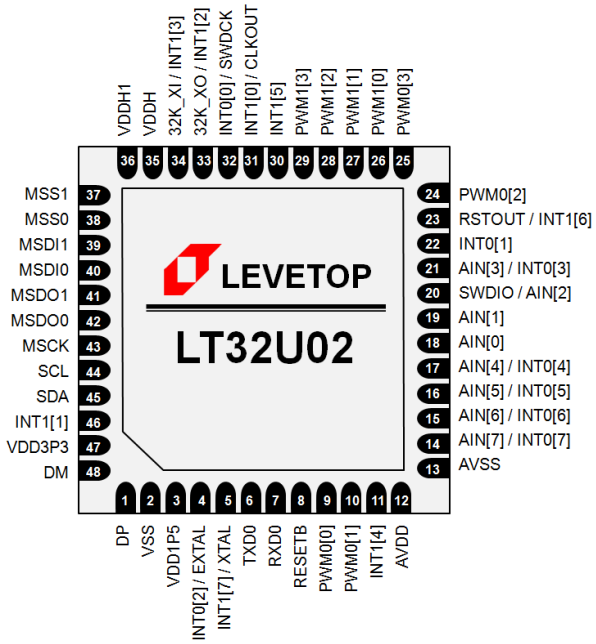

Figure 1: LT32U02

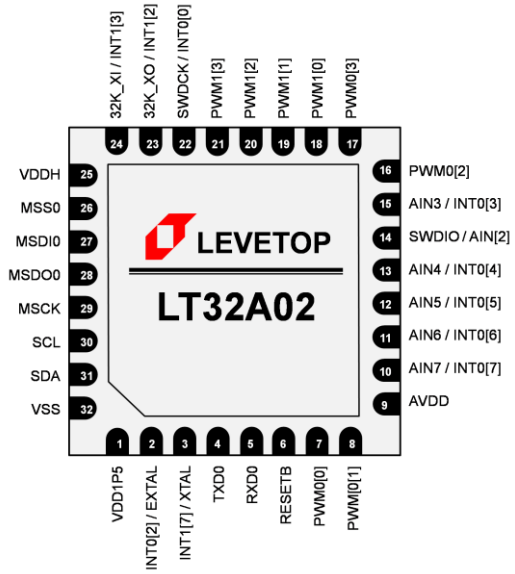

Figure 2: LT32A02

Features

C0 Processor

_ 32-bit Load/Store Reduced Instruction set Computer (RISC) Architecture with fixed 16-bit Instruction Length
_ 16 Entry 32-bit General-Purpose Register File
_ Efficient 3-Stage Execution Pipeline, Hidden from Application Software
_ Single-cycle Instruction Execution for many Instructions, Three Cycles for Branches
_ Support for Byte / Half-word / Word Memory Accesses
_ Embedded Interrupt Controller, support Nested Vector Interrupts.
_ Single-cycle 32-bit x 32-bit Hardware Integer Multiplier Array
_ 3~13 Cycles Hardware Integer Divider Array

8K Bytes of Static Random-Access Memory (SRAM)

_ Single Cycle Byte, Half-word (16-bit), and Word (32-bit) Reads and Writes

64K Bytes Embedded Flash (EFLASH)

_ Page Erase Capability: 512 bytes per Page
_ Read Cycle Time: 40ns (min)
_ Endurance: 100000 Cycles (min)
_ Greater than 20 Years Data Retention
_ Fast Page Erase/ Byte Program
  • Half-word Program Time: 7.5us (max)
  • Page Erase Time: 5 ms (max)
  • Mass Erase Time: 40 ms (max)
_ Single Cycle Byte, Half-word (16-bit) and Word (32-bit) Read Access.

Reset

_ Internal power on reset circuit
_ Five sources of reset:
  • Power-on Reset
  • External Pin
  • Software Reset
  • Watchdog Timer
  • Program Voltage Detect Reset
_ Status Flag Indicates Source of Last Reset

Four Periodic Interval Timer

_ 16-bit Counter with Modulus "initial count" Register
_ Selectable as Free Running or Count down
_ 16 Selectable Prescalars → 2^0 to 2^{15}

Two Watchdog Timer

_ 16-bit Counter with Modulus "Initial Count" Register
_ Pause Option for Low-power Modes
_ Up to 2000ms Service Time

Two External Interrupts Port (EPORT)

_ Eight Channels for Each EPORT
_ Rising/falling Edge Select
_ Low/High-Level Sensitive
_ Interrupt Pins Configurable as General-purpose I/O

Two Serial Peripheral Interface Master Module (SPI)

_ SPI Master Mode
_ Shared SPICLK Ports
_ Two 4 Entries deep Read FIFO
_ Two 4 Entries deep Write FIFO
_ Interrupt Generation after 1, 2, 3, or 4 Transferred Bytes
_ MSB/LSB Selectable
_ Variable Baud-rate During Communication
_ Serial Clock with Programmable Polarity and Phase
_ 16/32 bit Transmit/Receive Data Width
_ Byte Re-order
_ Controllable Slave Select (spiss0/1) bit

One Serial Communications Interface Module (SCI)

_ Standard Mark/Space Non-Return-to-Zero (NRZ) format
_ The Baud Rate Divisor is a 22-bit Number Consisting of 16-bit Integer and 6-bit Fractional Part
_ Programmable 7-bit, 8-bit or 9-bit Data Format
_ Separately enabled Transmitter and Receiver
_ Separate Receiver and Transmitter Central Processor unit (CPU) Interrupt Requests
_ Programmable Transmitter Output Polarity
_ Two Receiver Wakeup Methods:
  • Idle Line Wakeup
  • Address Mark Wakeup
_ Interrupt-driven Operation with Eight Flags:
  • Transmitter Empty
  • Transmission Complete
  • Receiver Full
  • Idle receiver Input
  • Receiver Overrun
  • Noise Error
  • Framing Error
  • Parity Error
_ Receiver Framing Error Detection
_ Hardware Parity Checking
_ 1/16 bit-time Noise Detection
_ General-purpose, I/O Capability
_ Serial IR Interface Low-speed, IrDA-Compatible (up to 115.2Kbit/s)

One USB2.0 Full Speed Compatible Device (LT32U02 Only)

_ Supports Internal Reference Clock or External 12MHz Crystal Reference Clock
_ Compliant with USB2.0 Full Speed Specification with on-chip Integrated PHY Module
_ Supports FS (12Mbps) Mode
_ Up to 8 Endpoints Supported Including Endpoint 0
_ All Endpoints except Endpoint 0 can support Interrupt and Bulk Transfer
_ All Endpoints except Endpoint 0 can be Configured as 8, 16, 32, 64 bytes FIFO size
_ Endpoint 0 Support Control Transfer

■ Two Pulse Width Modulator (PWM)

_ Four Channel each PWM Controller
_ Programmable Period
_ Programmable Duty Cycle
_ Two Dead-Zone Generator
_ Capture Function
_ Pins can be Configured as General-purpose I/O

■ ADC with 8-Channel

_ High Performance
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- ADC Conversion Time: 1.0μs for 12-bit Resolution (1 MHz), 0.88μs Conversion Time for 10 bit Resolution, Faster Conversion times can be obtained by Lowering Resolution.
- Programmable Sampling Time
- Data Alignment with Built-in Data Coherency
- DMA Support

_ Low Power
- Application cans Reduce PLCK Frequency for Low Power Operation while still Keeping Optimum ADC Performance. For Example, 1.0μs Conversion Time is kept, whatever the Frequency of PCLK.
- Wait mode: Prevents ADC Overrun in Applications with Low Frequency PLCK
- Auto off mode: ADC is Automatically Powered Off Except during the Active Conversion phase. This Dramatically Reduces the Power Consumption of the ADC.

_ Analog Input Channels
- 8 External Analog Inputs
- 1 Channel for Internal Reference Voltage
- 1 Channel for Internal Temperature Sensor

_ Start-of-Conversion can be Initiated:
- By Software
- By Hardware Triggers with Configurable Polarity

_ Conversion Modes
- Can Convert a Single Channel or can Scan a Sequence of Channels.
- Single Mode Converts Selected Inputs once per Trigger
- Continuous Mode Converts Selected Inputs Continuously
- Discontinuous Mode

_ Interrupt Generation at the end of Sampling, end of Conversion, end of Sequence Conversion, and in case of Analog Watchdog or Overrun Events.
_ Analog Watchdog
_ Single-ended and Differential-input Configurations
- Converter uses an Internal Reference or an External Reference

■ Two Analog Comparators

_ Programmable Response Time
_ Programmable Hysteresis
_ Support Analog input Multiplexer with Nine Selection
_ Two Optional Outputs: Filtered or Asynchronous Output
_ Selectable Rising/Falling Edge Interrupt

PMU

_ Support 3.3V LDO (for USB PHY Power Supply) with Maximum Load Current 100mA
_ 3.3V LDO Support Power Down for Save Power Consumption
_ Support 1.5V LDO with Maximum Load Current 50mA
_ 1.5V LDO Support Four Mode: Normal, Lower power, High power

Programmable Voltage Detector

Internal Oscillator

_ 128KHz Oscillator Clock for Watchdog and PMU
_ 72MHz Oscillator Clock which can be used for System Clock
_ 48MHz USBPLL Clock which can be used for System Clock

External Crystal Oscillator

_ Up to 20Mhz External Crystal Oscillator Clock which can be used for System Clock
_ 32.768Khz External Crystal Oscillator Clock which can be used for Watchdog

Block Diagram

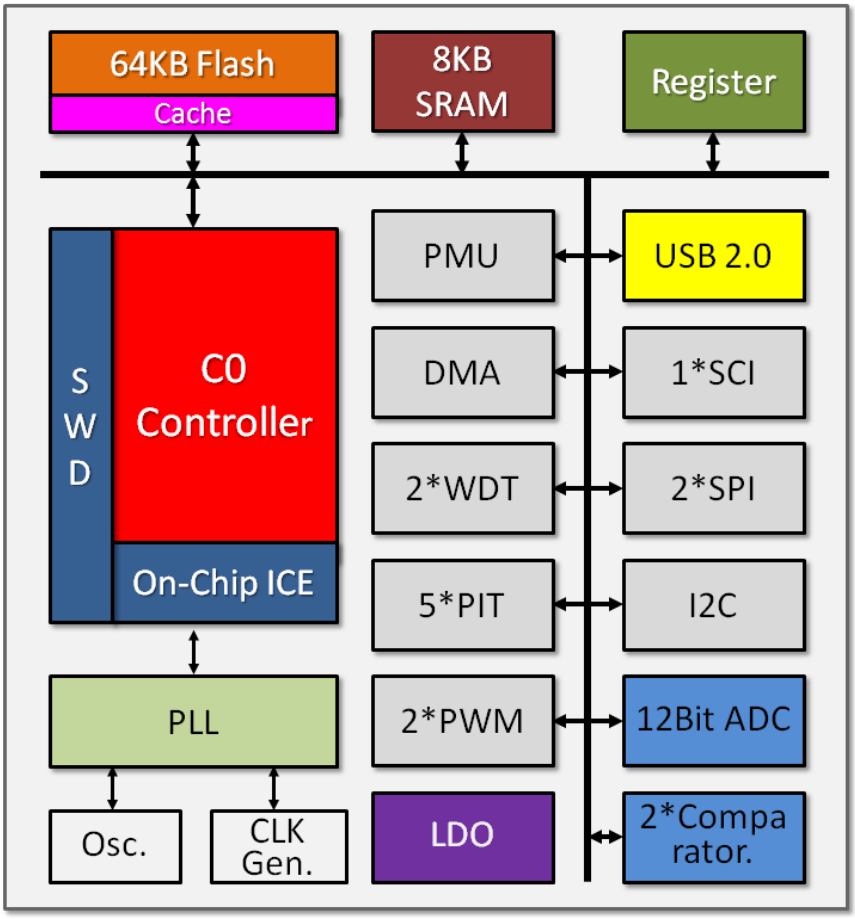

Figure 3: Block Diagram

Signal Properties Summary

Table 1: Signal Properties Summary

Name	Alternate	Qty.	Dir.	Input Sync	Pullup[1]	Output Drive (ST/OD/SP)[2]
SCI (2)						
RXD0		1	I/O	N	Pull-up	ST
TXD0		1	I/O	N	Pull-up	ST
USB (2)						
DP		1	Analog			SP
DM		1	Analog			SP
I2C (2)						
SCL		1	I/O	N	Pull-up	OD
SDA		1	I/O	N	Pull-up	OD
SPI (7)						
MSS0		1	I/O	N	-	ST
MSDI0		1	I/O	N	Pull-up	ST
MSDO0		1	I/O	N	-	ST
MSS1		1	I/O	N	-	ST
MSDI1		1	I/O	N	Pull-up	ST
MSDO1		1	I/O	N	-	ST
MSCK		1	I/O	N	-	ST
PWM0 (4)						
PWM0[0]		1	I/O	N	Pull-up	ST
PWM0[1]		1	I/O	N	Pull-up	ST
PWM0[2]		1	I/O	N	Pull-up	ST
PWM0[3]		1	I/O	N	Pull-up	ST
PWM1 (2)						
PWM1[0]		1	I/O	N	Pull-up	ST
PWM1[1]		1	I/O	N	Pull-up	ST
PWM1[2]		1	I/O	N	Pull-up	ST
PWM1[3]		1	I/O	N	Pull-up	ST
ADC (7)						
AIN[7:3]	INT0[7:3]	5	Mixed	N	-	-
AIN[1:0]	-	2	Analog	N	-	-
Edge Port 1 (5)						
INT1[1]		1	I/O	N	Pull-up	ST
INT1[2]	32K_XO	1	I/O	N	Pull-up	ST
INT1[3]	32K_XI	1	I/O	N	Pull-up	ST
INT1[4]		1	I/O	N	Pull-up	ST
INT1[5]		1	I/O	N	Pull-up	ST

Table 1: Signal Properties Summary (Continued)

Name	Alternate	Qty.	Dir.	Input Sync	Pullup[1]	Output Drive (ST/OD/SP)[2]
Edge Port 0 (1)						
INT0[1]	-	1	I/O	N	Pull-up	ST
Debug Port (2)						
SWDIO	AIN[2]	1	I/O	N	Pull-up	ST
SWDCK	INT0[0]	1	I/O	N	Pull-up	ST
Clock (3)						
EXTAL	INT0[2]	1	I/O	N	-	SP
XTAL	INT1[7]	1	I/O	N	-	SP
CLKOUT	INT1[0]	1	I/O	N	Pull-up	ST
RESET (2)						
RESETB	-	1	-	Y	-	SP
RSTOUT	INT1[6]	1	I/O	N	Pull-up	ST
Power Supply						
VDDH	-	-	-	-	-	SP
VDDH1	-	-	-	-	-	SP
VDD3P3	-	-	-	-	-	SP
VDD1P5	-	-	-	-	-	SP
VSS	-	-	-	-	-	SP
AVDD	-	-	-	-	-	SP
AVSS	-	-	-	-	-	SP

Notes:

1. All Pull-ups are disconnected when the signal is programmed as an output.
2. Output Driver Type: ST=Standard, SP=Special, OD=Standard Driver with Open-Drain Pull down option selected.

Signal Descriptions

Table 2: Signal Descriptions

Pin Name	Pin Number		Pin Description
	LT32U02	LT32A02	
RXD0	7	5	**Receive Data** This is a Serial Communications Interface 0 Module Signal (SCI0). This signal is used for the SCI receiver data input and is also available for GPIO when not configured for receiver operation.
TXD0	6	4	**Transmit Data** This is a Serial Communications Interface 0 Module Signal (SCI0). This signal is used for the SCI transmitter data output and is also available for GPIO when not configured for transmitter operation.
DP	1	--	**USB Data Positive** These signals are used by the USB module.
DM	48	--	**USB Data Negative** These signals are used by the USB module.
SCL	44	30	**I2C Clock** This signal is used for the I2C clock line signal and is also available for GPIO when not configured for receiver operation.
SDA	45	31	**I2C Data** This signal is used for the I2C data line signal and is also available for GPIO when not configured for transmitter operation.
MSDO0	42	28	**Master 0 Out** This signal is the serial data output from the SPI0 in master mode.
MSDO1	41	--	**Master 1 Out** This signal is the serial data output from the SPI1 in master mode.
MSDI0	40	27	**Master 0 In** This signal is the serial data input to the SPI0 in master mode.
MSDI1	39	--	**Master 1 In** This signal is the serial data input to the SPI1 in master mode.

Table 2: Signal Descriptions (Continued)

n Name	Pin Number		Pin Description
	LT32U02	LT32A02	
MSCK	43	29	**Master Serial Clock** The serial clock synchronizes data transmissions between master and slave devices. MSCK is an output and is shared between with SPI0 and SPI1.
MSS0	38	26	**Slave Select 0** This output signal is the peripheral chip select signal in master mode.
MSS1	37	--	**Slave Select 1** This output signal is the peripheral chip select signal in master mode
INT0[7]	14	10	**Edge Port 0 Signals** These bidirectional signals function as either external interrupt sources or GPIO.
INT0[6]	15	11	
INT0[5]	16	12	
INT0[4]	17	13	
INT0[3]	21	15	
INT0[2]	4	2	
INT0[1]	22	--	
INT0[0]	32	22	
INT1[7]	5	3	**Edge Port 1 Signals** These bidirectional signals function as either external interrupt sources or GPIO.
INT1[6]	23	--	
INT1[5]	30	--	
INT1[4]	11	--	
INT1[3]	34	--	
INT1[2]	33	--	
INT1[1]	46	--	
INT1[0]	31	--	
PWM0[3:0]	25,24,10,9	17,16,8,7	**Pulse Width Modulator 0 Signals** These out signals function as either PMW0 output or GPIO.
PWM1[3:0]	29,28,27,26	21,20,19,18	**Pulse Width Modulator 1 Signals** These out signals function as either PMW1 output or GPIO.

Table 2: Signal Descriptions (Continued)

Pin Name	Pin Number		Pin Description
	LT32U02	LT32A02	
AIN[7]	14	10	**Analog-to-Digital Converter Signals** These analog signals function as ADC analog channels.
AIN[6]	15	11	
AIN[5]	16	12	
AIN[4]	17	13	
AIN[3]	21	15	
AIN[2]	20	14	
AIN[1]	19	--	
AIN[0]	18	--	
SWDCLK	32	22	**Test Clock** This input signal is the test clock used to synchronize the SWD logic.
SWDIO	20	14	**Test Data Input / Output** This input/output signal is the serial input/output for test instructions and data.
EXTAL	4	2	**Fast Oscillator Pad Input** The signal is the input of fast Oscillator Pad.
XTAL	5	3	**Fast Oscillator Pad output** The signal is the output fast Oscillator pad.
32K_XI	34	24	**32.768Khz Oscillator Pad input** The signal is the input of 32.768Khz Oscillator Pad.
32K_XO	33	23	**32.768Khz Oscillator Pad output** The signal is the output 32.768Khz Oscillator pad.
CLKOUT	31	--	**Clock Out** This output signal reflects the internal system clock.
RESETB	8	6	**Reset In** This active-low input signal is used as the external reset request. Reset places the CPU in supervisor mode with default settings for all register bits except some register bits only reset by POR. 0 = external reset assert 1 = external reset desert

Table 2: Signal Descriptions (Continued)

Pin Name	Pin Number		Pin Description
	LT32U02	LT32A02	
RSTOUT	23	--	**Reset Out** This active-low output signal is an indication that the internal reset controller has reset the chip. 0 = chip is at reset status 1 = chip is not reset status
VDDH	35	25	**Power** This signal supplies 2.5~5.5V positive power to the I/O pads and LDO.
VDDH1	36	--	**Power** This signal supplies 2.5~5.5V positive power to the SPI I/O pads. VDDH1 is short together with VDDH in QFN32 package.
VDD3P3	47	--	**Power** 3.3V LDO output signal and is used to supply the power of USB transceiver. 1uF ceramic bypass capacitor is required to externally connect between the pad and vss.
VDD1P5	3	1	**Core Power** 1.5V LDO output signal and is used to supply the power of the core logic. 1uF ceramic bypass capacitor is required to externally connect between the pad and vss.
VSS	2	32	**Ground** This signal supplies 2.5~5.5V negative supply (ground) to the I/O pads and LDO.
AVDD	12	9	**Analog Power** This signal supplies 2.5~5.5V positive power to analog module.
AVSS	13	--	**Analog Ground** This signal is the negative supply to the Analog module.

Notes:

1. The SPI signals are used by the SPI modules and may also be configured to be discrete I/O signals.
2. The VDD and VSS signals provide system power and ground to the chip. Multiple signals are provided for adequate current capability. All power supply signals must have adequate bypass capacitance for high-frequency noise suppression.

Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it. See Table 3. The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, either V_{SSH} or V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings. Refer to "DC Electrical Specifications" for guaranteed operating conditions.

Table 3: Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	V_{ddh}	-0.5 to +5.5	V
2	Supply Voltage	V_{ddh1}	-0.5 to +5.5	V
3	Input Voltage[1]	Avdd	-0.5 to +5.5	V
4	Operating Temperature Range	TOPT	-40 to +85	^{O}C

DC Electrical Specifications

Table 4: DC Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{ddh}	2.0 (LT32A02) 2.8 (LT32U02)	3.3/5.0	5.5	V
Input High Voltage	V_{IH}	0.65*V_{ddh}	-	V_{ddh}	V
Input Low Voltage	V_{IL}	V_{SS}	-	0.35*V_{ddh}	V
Output High Voltage	V_{OH}	0.8*V_{ddh}	—	—	V
Output Low Voltage	V_{OL}	—	—	0.1*V_{ddh}	V
Pull-Up Resistor	R_{PU}	20		100	Kohm
Pull-Down Resistor	R_{PU}	20		100	Kohm
Low Level Output Current @ V_{OL}=0.1*V_{ddh}	I_{OL}			6	mA
High Level Output Current @ V_{OH}=0.8*V_{ddh}	I_{OH}			6	mA