乐升半导体
LEVETOP

LT2305

電容式觸控螢幕控制芯片

Capacitive Touch Screen Controller

Introduction

LT2305 is a 60-channel analog-front-end capacitive touch controller for multi-touch screen applications. LT2305 adopted with configurable sensing architecture and extensible serial bus interfaces, and the sensing and driving channels of touch sensing system can be extend for different applications by parallel connection of multiple chips. LT2305 is designed based on a patent touch sensing technology named as touch prediction and window sampling (TPWS) technology, and 4 parallel CDCs (Capacitance to Digital Converters) were built in for high speed, low cost and low power capacitive touch screen applications.

LT2305 can run with SPI interface of clock frequency up to 500KHz for capacitance measurements under 2.8V ~ 5.5V, -40℃ ~ 85℃.

Package Types

LT2305A
QFNWB8x8-68L

LT2305B
QFNWB6x6-48L

Features

- 60-channel Configurable Sensor Channels.
- Built-in 4 Parallel Capacitance to Digital Converters.
- Configurable Sensing Architecture and Extensible Serial Bus Interface.
- Programmable Electrodes Sensing and Driving Sequential.
- Wide Ranged Power Supply from 2.8V to 5.5V.
- Ultra Low Power Consumption in Active Mode and Standby Mode.
- Excellent Noise Suppression Capability.
- Accommodating with Large Resistance of Lines
- Provide QFN68L, QFN48L Packages.

Model

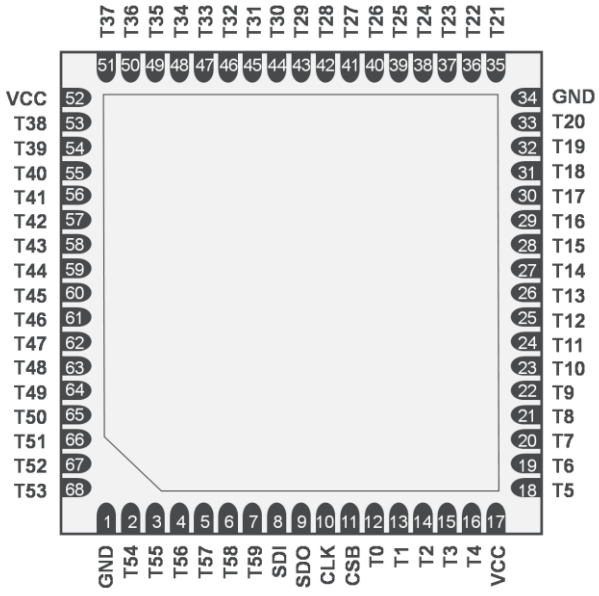
Model	Package	Application
LT2305A	QFNWB8x8-68L	Max. 60 channels
LT2305B	QFNWB6x6-48L	Max. 42 channels

Pin Description

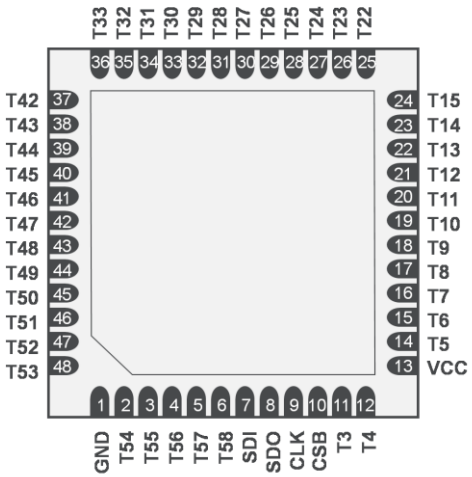
*Pin No. (LT2305A)	Pin Name	I / O	Descriptions
9	SDO	O	SPI Data Output
8	SDI	I	SPI Data Input
10	CLK	I	SPI Clock Input
11	CSB	I	SPI Chip Select Input
12~16, 18~33, 35~51, 53~68, 2~7	T0~T59	I/O	Sensor Channels Connected with Touch Screens
1, 34	GND	PWR	Ground Pins
17, 52	VCC	PWR	Power Supply

*Note: The Pin number of above table is base on LT2305A. The pin number of pin name are difference for each part number. Please refer to the pin assignment of below diagrams.

Pin Assignment

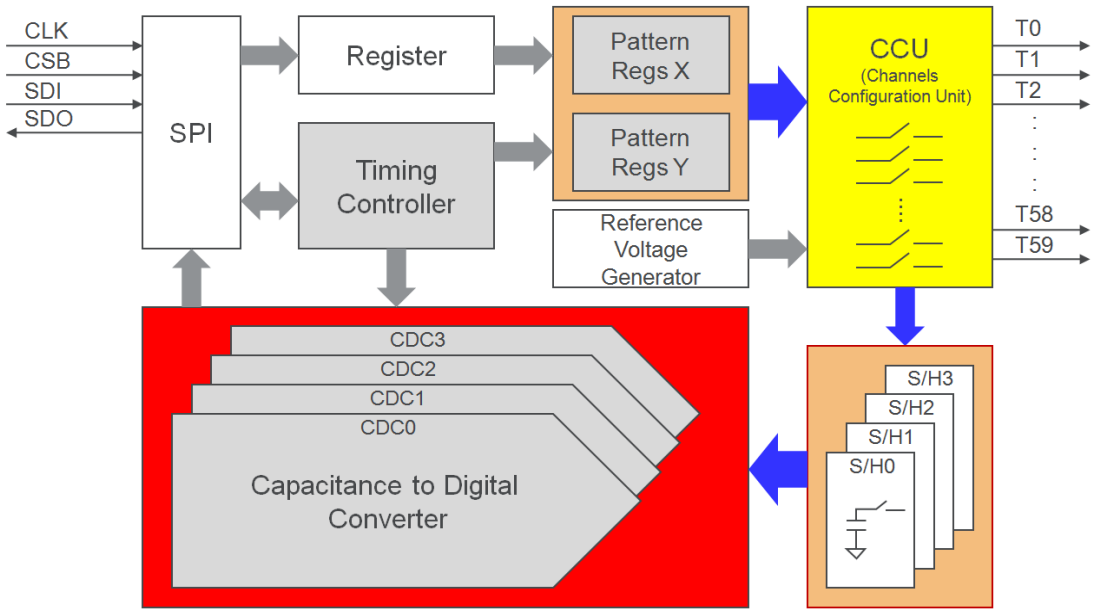


LT2305A

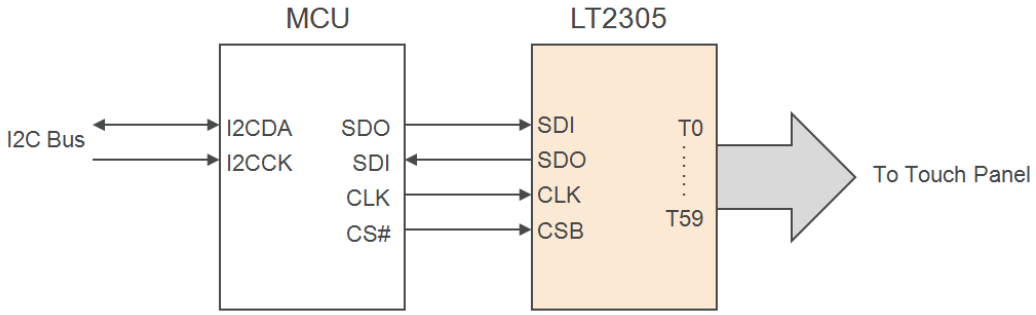


LT2305B

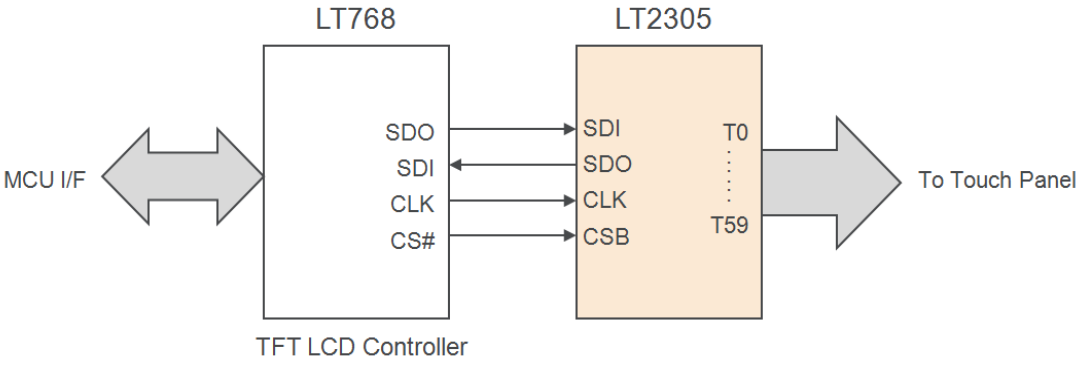
Internal Block Diagram



Application Block Diagram



The Application Circuit of Multi-point Capacitive Touch Screen



The Combination Circuit of LT2305 and LT768x

Absolute Maximum Ratings

Symbol	Descriptions	Value	Unit
VCC	Power Supply Voltage	-0.3 ～ 6	V
V_I	IO Input	-0.3 ～ VCC+0.3	V
V_O	IO Output	-0.3 ～ VCC+0.3	V
S	Sensor Channels	-0.3 ～ VCCA+0.3	V
T_{OPR}	Operating Temperature	-40 ℃ to 85 ℃	℃
T_{STG}	Storage Temperature	-55 ℃ to 150 ℃	℃

Note: If used beyond the absolute maximum ratings, LT2305 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

Electrical Characteristics (Condition: Vcc=3.3V, T_A=25℃)

Symbol	Item	Test Condition	Min.	Typ.	Max.	Unit
VCC	Power Supply		2.8		5.5	V
VIH	IO Input High		0.7VCC		VCC+0.3	V
VIL	IO Input Low		-0.3		0.3VCC	V
IL	Input Leakage	VCC=5V		127		uA
		VCC=3.3V		51.6		uA
VOH	IO Output High	IOH=-2mA	2.4			V
VOL	IO Output Low	IOH=2mA			0.4	V
Cm	Sensor Resolution			8.8		fF
Is	Standby Current	VCC=3.3V CSB=H		7		uA
IOP	Operation Current	VCC=3.3V CSB=L		6		mA

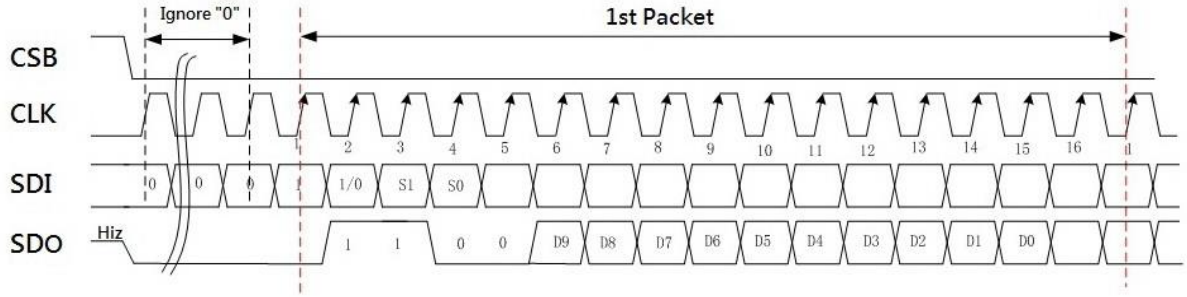
Function Description

1. SPI Interface

The LT2305 latches input data (SDI) on rising edge of clock (CLK). Data out (SDO) is changed during falling edge of the clock.

The LT2305 communication relies on packets of 16bits. The CSB pin must be kept low during the full command transmission, which can span over several packets. When the chip select signal is activated (CSB pin falling edge), the LT2305 starts to sample the SDI pin on each rising edge of CLK. The CSB pin has to stay low for the whole command/data transmission period. With CSB=0, the first bit that is taken into account has to be a logic 1.

All incoming bits with logic 0 arriving prior the logic 1 are ignored. The first bit at logic 1 is part of the first packet (first bit of 16bits packet) and acts as synchronization bit. Once it is synchronized, the LT2305 keeps tracking the packet positions using a clock counter. Each group of 16 clock pulses defines a new packet. The following packets are not re-synchronized and solely relied on the initial alignment. The host can verify that the synchronization is still valid by checking that each reply packet starts with a pattern of two-bit 1 followed by two-bit 0.



The LT2305 supports two types of communication packets. One is command packet, which is used to update analog-front-end control registers and pin configuration registers. Another is the index packet, which is used to update the command pointer. The type of communication packets is defined by the bit after synchronization bit (the second bit of a 16bits packet). Logic 1 defines an index packet, and logic 0 defines a command packet.

All SPI interface logic and registers of the LT2305 will be reset when the CSB is set to 1. The analog-front-end control registers and pin configuration register, data register data are kept unchanged as long as the power supply is maintained. The reset is released as soon as CSB is set to 0.

2. Register Tables

Index	W/R	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP	W	1	1	-	-	-	-	-	IREN	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
Setup Configuration																	
0x01	W	1	0	PKG[1:0]		CF	SADDR[5:0]										
Pattern Configuration																	
0x02	W	1	0	TX[1:0]		Tstart[5:0]						Tend[5:0]					
0x03	W	1	0	AE0	AE1	AE2	AE3	PS[1:0]		SAoffset[3:0]				RAoffset[3:0]			
0x04	W	1	0	AA1	AA0	SA[5:0]						RA[5:0]					
Internal Capacitors Configuration																	
0x05	W	1	0	TC0_EN	TC0_TC[2:0]		TC0_BC[1:0]		TC0[3:0]					ASRE0			
0x06	W	1	0	TC1_EN	TC1_TC[2:0]		TC1_BC[1:0]		TC1[3:0]					ASRE1			
0x07	W	1	0	TC2_EN	TC2_TC[2:0]		TC2_BC[1:0]		TC2[4:0]						ASRE2		
0x08	W	1	0	TC3_EN	TC3_TC[2:0]		TC3_BC[1:0]		TC3[4:0]						ASRE3		
0x09	W	1	0	TC4_EN	TC4_TC[2:0]		TC4_BC[1:0]		TC4[4:0]						ASRE4		
0x0A	W	1	0	TC5_EN	TC5_TC[2:0]		TC5_BC[1:0]		TC5[4:0]						ASRE5		

Index		W/R	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Measurements Configuration																		
0x0B		W	1	0	ME	A_SEL	PL	GS	MU_EN[3:0]				CHOPE		ITY	ASIBY		OEB
Probe & Data Output Configuration																		
0x0C		W	1	0	PB10[1:0]		PB11[1:0]		PB12[1:0]		PB13[1:0]		PRM[1:0]		S[1:0]		PCL[1:0]	
0x0D	Packet1	W	1	0	S[1:0]		PCL[1:0]		PRM[1:0]		TC0_EN	TC1_EN	TC2_EN	TC3_EN	TC4_EN	TC5_EN		
		O	1	1	0	0	D*9	D*8	D*7	D*6	D*5	D*4	D*3	D*2	D*1	D*0	-	-
	Packet2	W	1	0				-	-	-	-	-	-	-	-	-	-	-
		O	1	1	0	0	D*9	D*8	D*7	D*6	D*5	D*4	D*3	D*2	D*1	D*0	-	-
	Packet3	W	1	0				-	-	-	-	-	-	-	-	-	-	-
		O	1	1	0	0	D*9	D*8	D*7	D*6	D*5	D*4	D*3	D*2	D*1	D*0	-	-
	Packet4	R	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		O	1	1	0	0	D*9	D*8	D*7	D*6	D*5	D*4	D*3	D*2	D*1	D*0	-	-

3. Register Description

3.1 Command Pointer (CP Register)

The CP register is used to storage the command pointer and the command pointer update control bit. The CP register can only be accessed by write the 16bits index communication packet.

The "IR[7:0]" is the command pointer, which point to the control registers. The "IREN" is command pointer automatic update enable or disable. When IREN=0, the command pointer automatic update disabled; When IREN=1, the command pointer automatic update enabled; If the function of command pointer automatic update enabled, the command pointer "IR[7:0]" will be automatically update by plus with 1 after an effective command packet write operation. If the function of command pointer automatic update disabled, the command index pointer "IR[7:0]" can only be update by write the 16bits index communication packet.

When IREN=1, the command pointer automatic update will stop at 0x0D.

3.2 Setup Configuration Registers (0x01)

Command 01: This command is used to set the information of chip package and pattern segmentation.

PKG[1:0]: The chip package type configurations.

PKG[1:0]	Package	Sensor Pins
00	QFN68L	T0~T59
11	QFN48L	T3~T15, T22~T33, T42~T58

CF: The pattern segmentation Enable/Disable.

0: The pattern segmentation disabled. All sensor pins configured by PKG[1:0] will be load/shift/hold as single group.

1: The pattern segmentation enabled. All sensor pins configured by PKG[1:0] will be divided into two groups (X segmentation and Y segmentation). Sensor pins in different groups can be load/shift/hold independently.

DSAE: Enable/Disable the only measurement pin setting.

1: Enable.

0: Disable.

SADDR[5:0]: The pattern segmentation pointer. When CF=1, the sensor pins from 0 to SADDR[5:0] will be configured as X segmentation, and sensor pins from SADDR[5:0]+1 to 59 will be configured as Y segmentation.

Note: When CF=1, the SADDR[5:0] should point to a valid Sensor Pins defined by PKG[1:0].

3.3 Pattern Configuration Registers (0x02~0x04)

3.3.1 The Drive Pattern Configuration (0x02)

Command 02: This command is used to set the sensor pins from Tstart[5:0] to Tend[5:0] with drive pattern TX[1:0].

TX[1:0]: The drive pattern mode.

TX[1:0]	Sensor Pins
00	GND
01	Lift Positive
10	Lift Negative
11	Floating

Tstart[5:0]: The sensor pins will be set with drive pattern start address.

Tend[5:0]: The sensor pins will be set with drive pattern end address.

3.3.2 The Measurement Pattern Configuration (0x03)

Command 03: This command is used to set the measurement pattern priority level, configuration mode, and the offset address when define the measurement units in group operation.

AE3, **AE2**, **AE1**, **AE0**: The measurement pattern of CDC3, CDC2, CDC1, CDC0 priority level setup.

1: The measurement pattern has higher priority level than drive pattern. The specified sensor pins will be set by measurement pattern instead of drive pattern.

0: The measurement pattern has lower priority level than drive pattern. The specified sensor pins will be set by drive pattern instead of measurement pattern.

PS[1:0]: The measurement pattern group configuration.

00: The CDC3, CDC2, CDC1, CDC0 is set as four independent groups, and the measurement pattern set by command 07 independently.

01: The CDC0 and CDC1 are set as a group. Use command 07 set sense line and reference line of CDC0 (SA[5:0], RA[5:0]), the sense line of CDC1 is set by SA[5:0] + SAoffset[3:0], the reference line of CDC1 is set by RA[5:0] + RAoffset[3:0] automatically.

10: The CDC0, CDC1, CDC2 measurement pattern set as a group. Use command 07 set sense line and reference line of CDC0 (SA[5:0], RA[5:0]).

The sense line of CDC1 is set by SA[5:0] + SAoffset[3:0], the reference line of CDC1 is set by RA[5:0] + RAoffset[3:0] automatically.

The sense line of CDC2 is set by SA[5:0]+ 2*SAoffset[3:0], the reference line of CDC2 is set by RA[5:0] + 2*RAoffset[3:0] automatically.

11: The CDC0, CDC1, CDC2, CDC3 measurement pattern set as a group. Use command 07 set sense line and reference line of CDC0 (SA[5:0], RA[5:0]).

The sense line of CDC1 is set by SA[5:0] + SAoffset[3:0]. The reference line of CDC1 is set by RA[5:0] + RAoffset[3:0] automatically.

The sense line of CDC2 is set by SA[5:0] + 2*SAoffset[3:0]. The reference line of CDC2 is set by RA[5:0] + 2*RAoffset[3:0] automatically.

The sense line of CDC3 is set by SA[5:0] + 3*SAoffset[3:0], the reference line of CDC3 is set by RA[5:0] + 3*RAoffset[3:0] automatically.

SAoffset[3:0]: Offset of Sense line.

RAoffset[3:0]: Offset of Reference line.

Command 04: This command is used to set the specified sensor pins as sense line and reference line.

AA1, **AA0**: The measurement unit (CDC0, CDC1, CDC2, CDC3) pointer.

AA1, AA0	Measurement Unit
00	CDC0
01	CDC1
10	CDC2
11	CDC3

SA[5:0]: Sense line address.

RA[5:0]: Reference line address.

Note:

(1) When ME=1, Reference line setting will be disable.

(2) Setting any two of measurement unit(CDC0, CDC1, CDC2, CDC3) to same sensor pins is not allowed, it will result in measure failure.

3.4 Internal Capacitors Configuration (0x05~0x0A)

TC5[4:0], TC4[4:0], TC3[4:0], **TC2[4:0]**, **TC1[3:0]**, **TC0[3:0]**: The internal capacitors value of TEcap5, TEcap4, TEcap3, TEcap2, TEcap1 and TEcap0.

TC2/3/4/5 [4:0]	TEcap2/3/4/5 (pF)
00000	0
00001	0.4
00010	0.8
00011	1.2
00100	1.6
00101	2.0
00110	2.4
00111	2.8
01000	3.2
01001	3.6
01010	4.0
01011	4.4
01100	5.8
01101	5.2
01110	5.6
01111	6.0
10000	6.4
10001	6.8
10010	7.2
10011	7.6
10100	8.0
10101	8.4
10110	8.8
10111	9.2
11000	9.6
11001	10.0
11010	10.4
11011	10.8
11100	11.2
11101	11.6
11110	12.0
11111	12.4

TC0/1 [3:0]	TEcap0/1 (pF)
0000	0
0001	0.4
0010	0.8
0011	1.2
0100	1.6
0101	2.0
0110	2.4
0111	2.8
1000	3.2
1001	3.6
1010	4.0
1011	4.4
1100	5.8
1101	5.2
1110	5.6
1111	6.0

TC5_EN, **TC4_EN,** **TC3_EN**, **TC2_EN**, **TC1_EN**, **TC0_EN**: The internal capacitor Enable/Disable control of Tecap5, Tecap4, TEcap3, TEcap2, TEcap1 and TEcap0.

1: Enable

0: Disable

TC5_TC[2:0], **TC4_TC[2:0]**, **TC3_TC[2:0]**, **TC2_TC[2:0]**, **TC1_TC[2:0]**, **TC0_TC[2:0]**: The Tecap5, Tecap4, TEcap3, TEcap2, TEcap1, TEcap0 top plate connection select.

TC1_TC[2:0]	TEcap1 Connection with
000	S0
001	R0
010	S1
011	R1
100	S2
101	R2
110	S3
111	R3

TC5_BC[1:0], **TC4_BC[1:0]**, **TC3_BC[1:0]**, **TC2_BC[1:0]**, **TC1_BC[1:0]**, **TC0_BC[1:0]**: The TEcap5, TEcap4, TEcap3, TEcap2, TEcap1, TEcap0 bottom plate connection select.

TC1_BC[1:0]	TEcap1 Connection with
00	Ground
01	LN
10	LP
11	Floating

ASRE0, ASRE1, ASRE2, ASRE3, ASRE4, ASRE5: When the Internal capacitor used for offset cancellation, set related ASRE* bit as 1.

3.5 Measurement Configuration (0x0B)

Command 0B: This is the command of measurement configuration.

ME: Measurement mode select.

1: Single input measurement.

0: Dual input differential measurement.

A_SEL: The convergence algorithm select.

1: The positive convergence algorithm selected.

0: The negative convergence algorithm selected.

PL: The measurements common input range select.

1: High level common input selected.

0: Low level common input selected.

GS: The measurements gain setting.

GS	CDC Resolution	Measurements Range (GM=1)
0	8.1fF	4.1pF
1	16.2fF	8.2pF

MU_EN[3:0]: The measurement unit(CDC0, CDC1, CDC2, CDC3) Enable/Disable control.

1: Enable.

0: Disable.

CHOPE: Chop enable/disable

1: Chop enable

0: Chop disable

ITY : The sensor channel initial configuration

1: Initial sensor channel to VCC.

0: Initial sensor channel to GND.

AS1BY: The amplifier stage 2 enable/disable

1: Disable the amplifier stage 2

0: Enable the amplifier stage 2

OEB :

0: The SPI SDO output data..

1: The SPI SDO output Hiz.

3.6 Probe & Data Output Configuration (0x0C~0xD)

Command 0C: This command is used to set the data output configuration and pattern shift mode.

PB10[1:0]: The first output packet (packet1) data select.

PB11[1:0]: The second output packet (packet2) data select.

PB12[1:0]: The third output packet (packet3) data select.

PB13[1:0]: The last output packet (packet4) data select.

PB**[1:0]	The Output Packet Data Select
00	CDC0 Output
01	CDC1 Output
10	CDC2 Output
11	CDC3 Output

PRM[1:0]: The active pattern group select.

PRM[1:0]	Pattern Shift Mode
00	When CF=1, X segmentation active. When CF=0, All sensor pins not disabled active.
01	When CF=1, Y segmentation active. When CF=0, All sensor pins not disabled active.
10	When CF=1, X &Y segmentation active. When CF=0, All sensor pins not disabled active.

S[1:0]: The active pattern group operation mode.

S[1:0]	The Active Pattern Group Operation Mode
00	The active pattern load
01	The active pattern hold
10	The active pattern shift increment
11	The active pattern shift decrement

Note: When CF=1, the inactive pattern will be in hold state.

PCL[1:0]: The length of current probe command.

PCL[1:0]	The Length of The Probe Command.
00	1 packet
01	2 packets
10	3 packets
11	4 packets

Command 0D: This is a probe command. The command length can be set by PCL[1:0]， and the pattern shift controlled by PRM[1:0] and S[1:0].

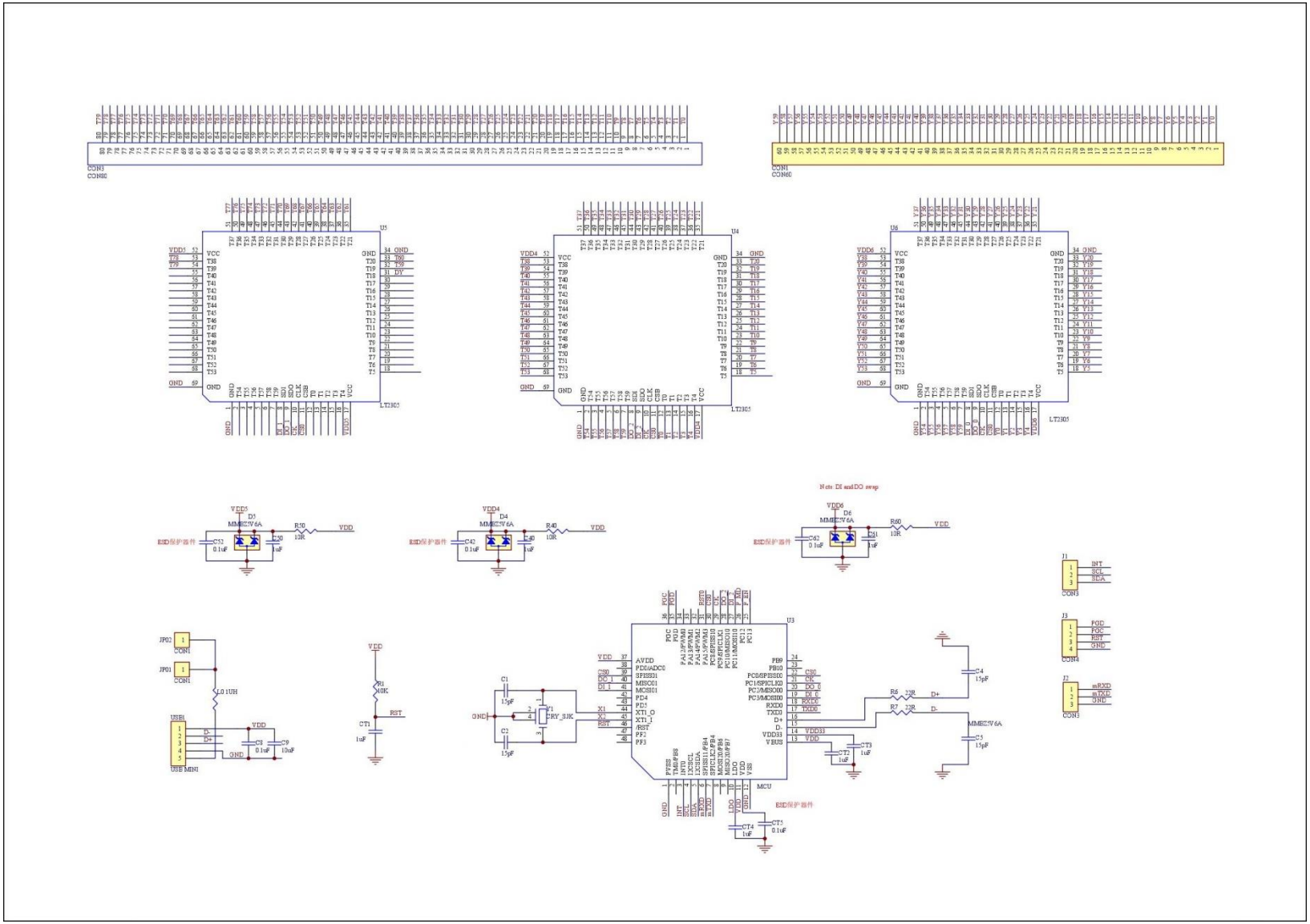
S[1:0]: The active pattern group operation mode, refer to command 0C, S[1:0] defined in command 0D is used to set pattern operation mode of next probe command.

PRM[1:0]: PRM[1:0] defined in command 0D is used to active pattern group select of the next probe command.

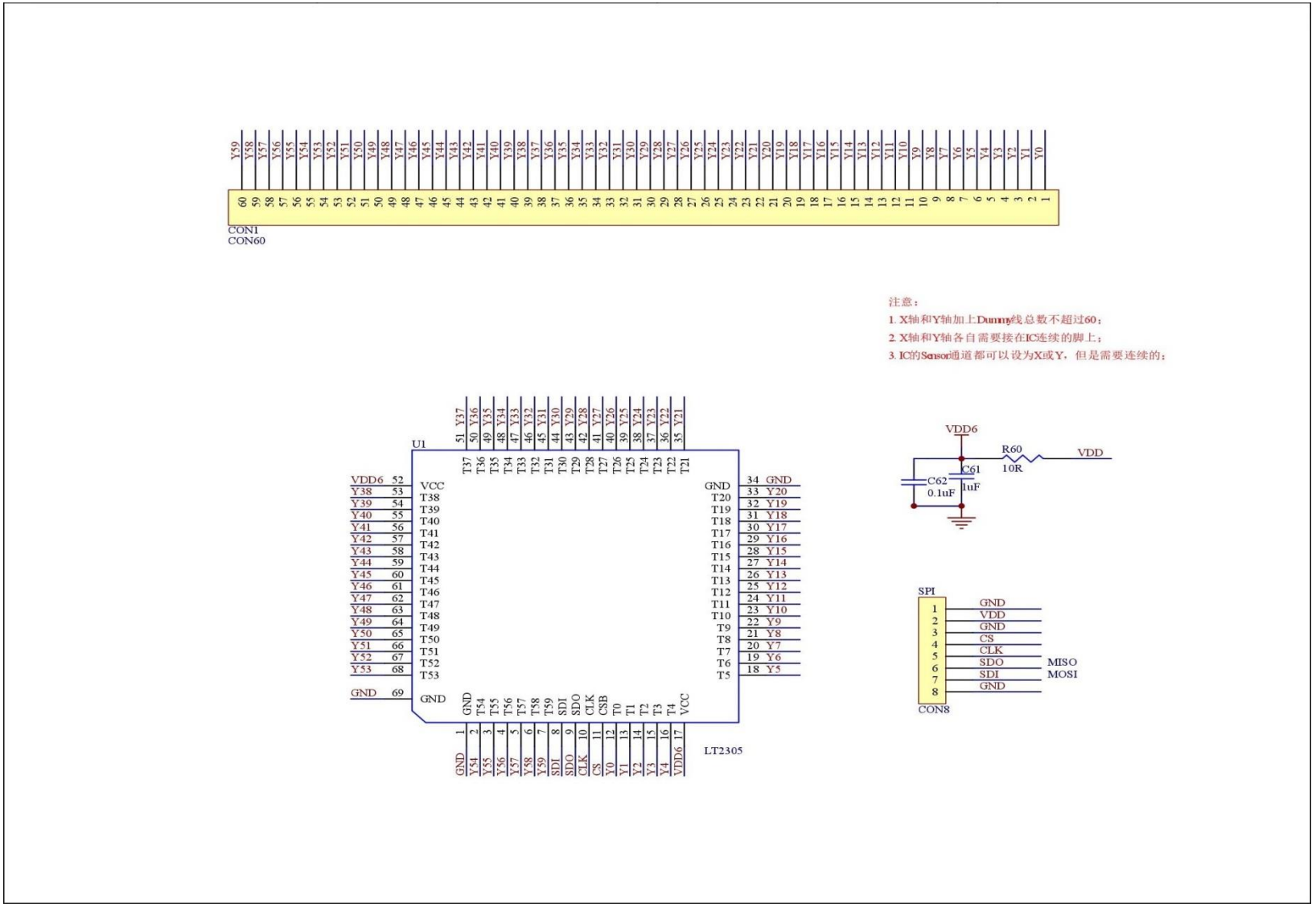
TC0_EN, **TC1_EN**, **TC2_EN**, **TC3_EN**, **TC4_EN**, **TC5_EN**: Enable or Disable of the internal capacitor connection of the next probe command.

PCL[1:0]: The length of current probe command. Refer to command 0C. PCL[1:0] defined in command 0D is used to set length of the probe command in next probe command.

4. .Application Circuit(1)

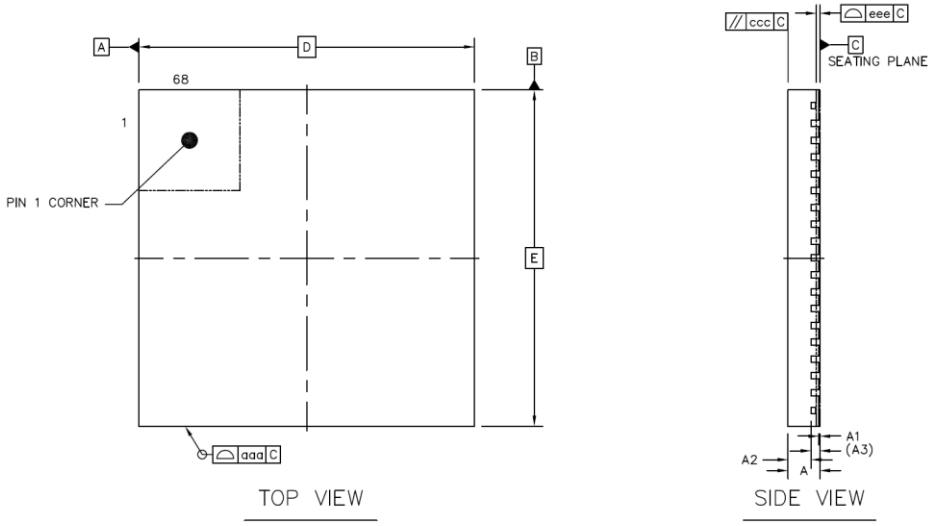


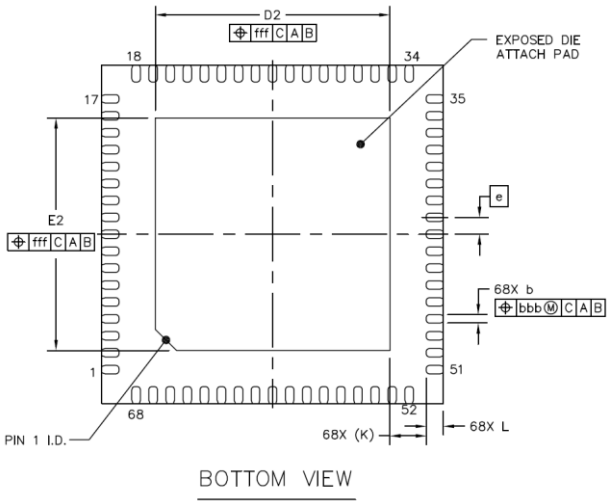
5. .Application Circuit(2)



Package Information

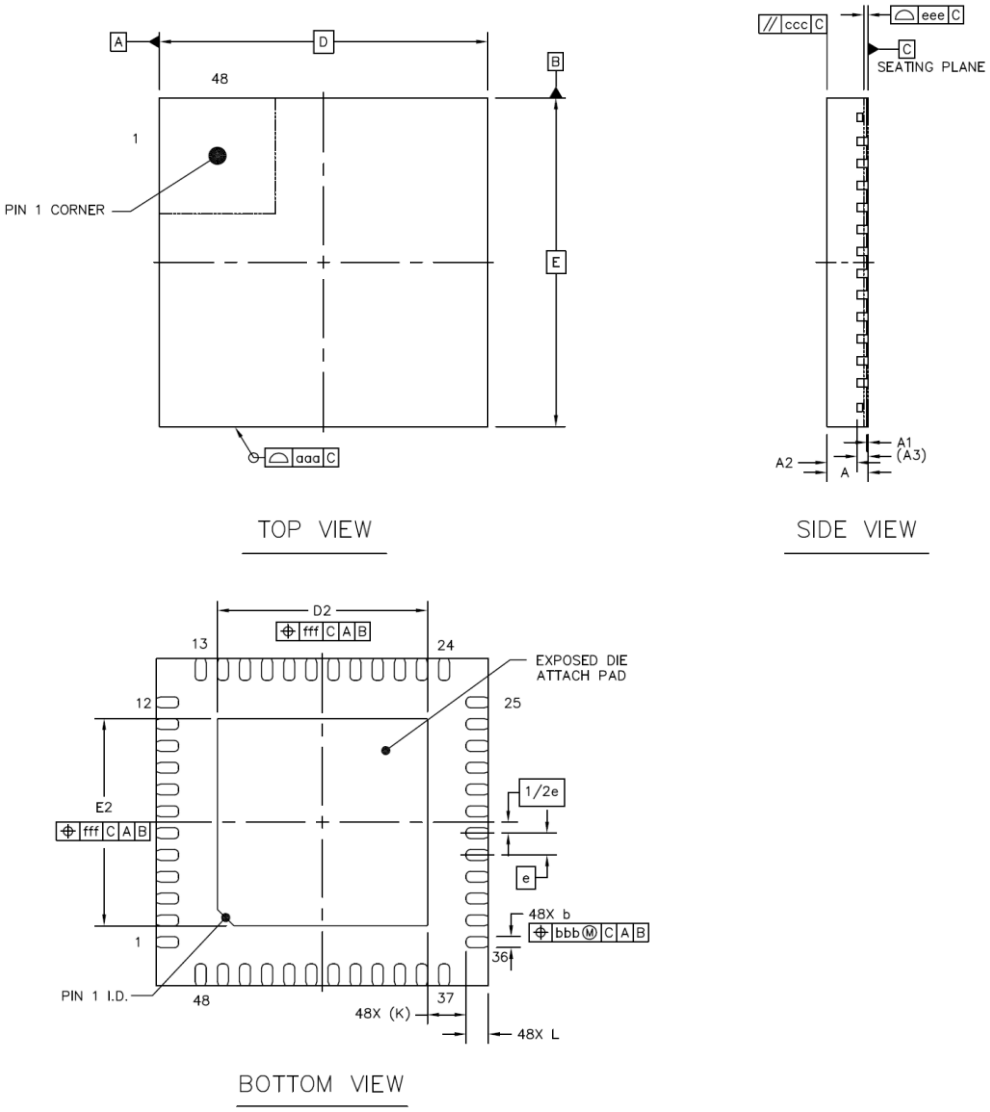
LT2305A (68Pin QFN)





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	5.4	5.5	5.6
	Y	E2	5.4	5.5	5.6
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.85 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

LT2305B (48Pin QFN)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.7	3.8	3.9
	Y	E2	3.7	3.8	3.9
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.7 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Revision

Version	Date	Description
V1.0	2017/10/17	Preliminary Version.
V0.9	2018/01/02	Update Model Name.

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